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# MS-7636 mATX Version: 3.1



## CPU:

INTEL - Lynnfield/ Clarkdale LGA 1156

## Main Memory:

Dual Channel DDRIII **x 2 (Max 16GB) (800 / 1066 / 1333/ 1600\* / 1800\* / 2133\*MHz)**

## System Chipset:

South Bridge : INTEL IBEXPEAK PCH (H55)

## On Board Chip:

Super I/O : FINTEK F71889ED  
 LAN : Realtek RTL8111E  
 HD Audio : Realtek ALC887 **colay ALC892**

## Expansion Slots:

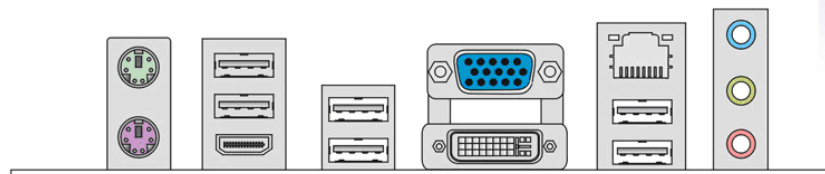
PCI-EPRESS X 16 SLOT **x 1**  
 PCI-EPRESS X 1 SLOT **x 2**

## PWM:

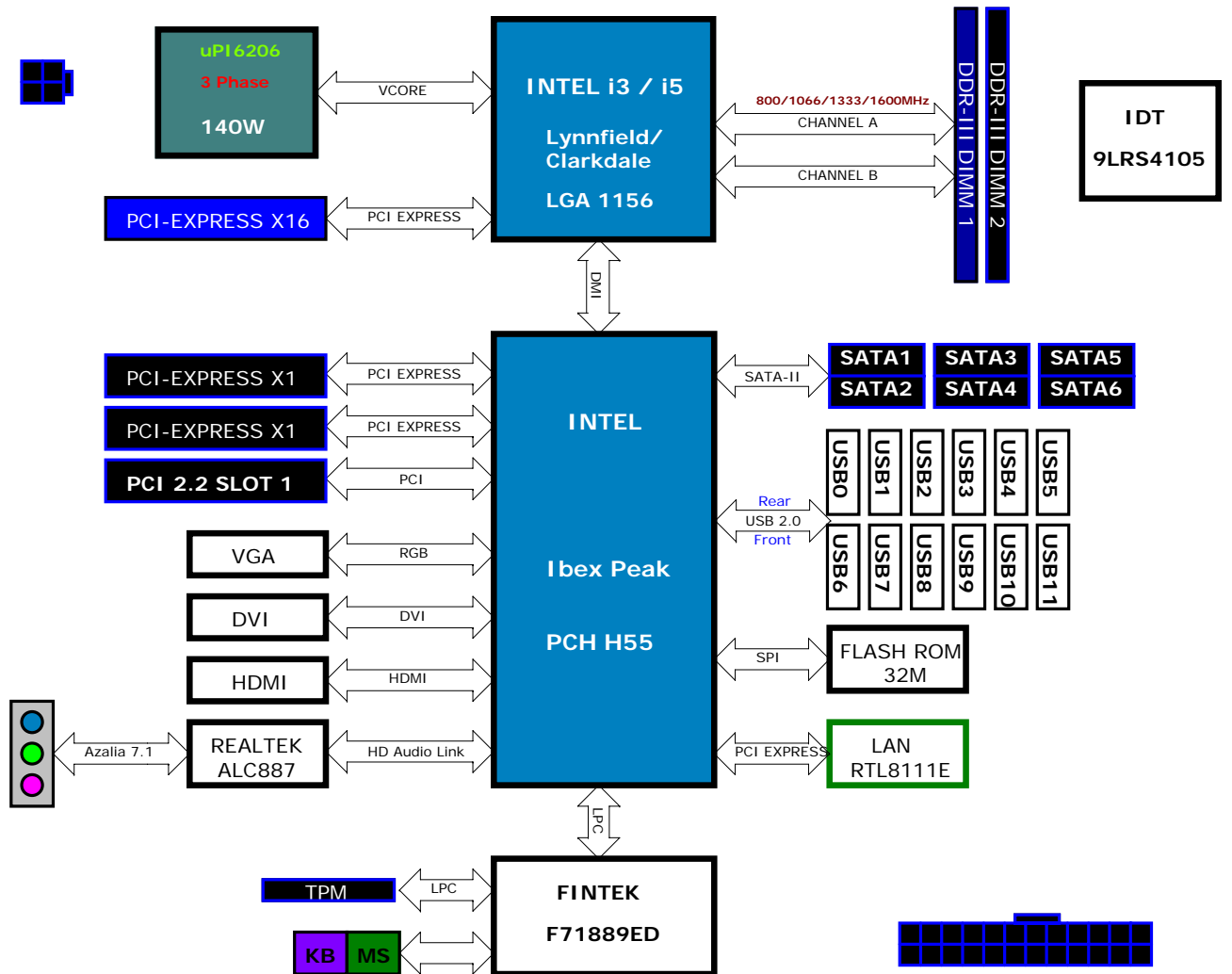
Controller : UPI uP6206 **(3 Phase / 125W)**

## Clock Generator:

Controller : IDT 9LRS4105

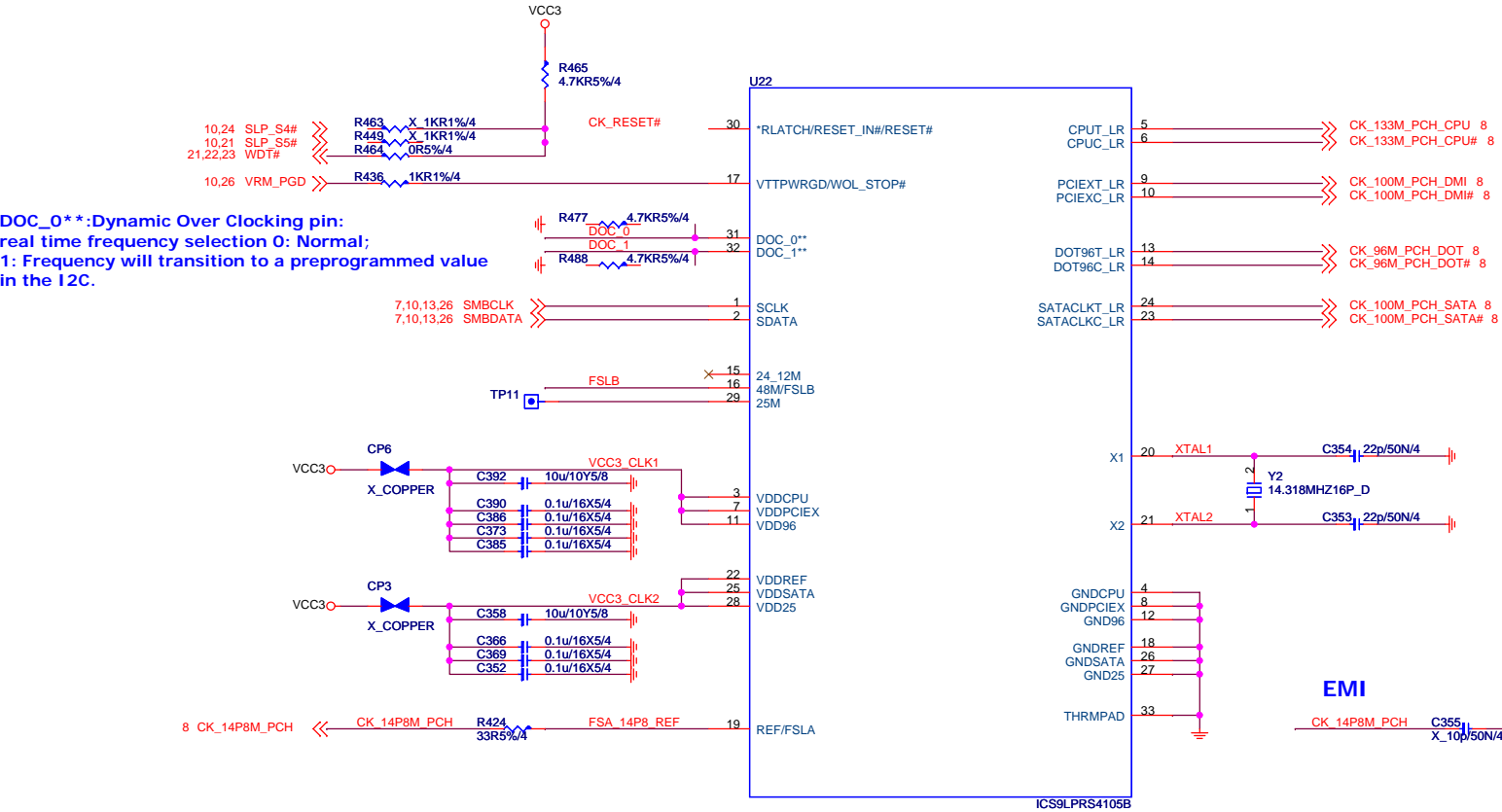


# Block Diagram



Bom Config	Audio	LAN	USB1	JUSB2/ JUSB3	APS LED	OC SW	CAP
Cfg-7636-30_A	892 / 6 PORT JACK	8111E (Gb LAN)	Y	Y	N	N	OSCON
Cfg-7636-30_B	887 / 3 PORT JACK	8105E(10/100)	N	Y	N	N	OSCON+EL
Cfg-7636-30_C	887 / 3 PORT JACK	8111E (Gb LAN)	N	N	N	N	OSCON
Cfg-7636-30_D							

CLK GEN ICS9LPRS4105B



DOC\_0\*\*:Dynamic Over Clocking pin:  
real time frequency selection 0: Normal;  
1: Frequency will transition to a preprogrammed value  
in the I2C.

EMI

CLOCK GEN STRAPING

FS4	FS3	FS2	FSB	FSA	CPU	Spread
B0b4	B0b3	B0b2	B0b1	B0b0	Mhz	%
0	0	0	0	0	100.00	-0.5
0	0	0	0	1	133.33	-0.5
0	0	0	1	0	200.00	-0.5
0	0	0	1	1	166.66	-0.5



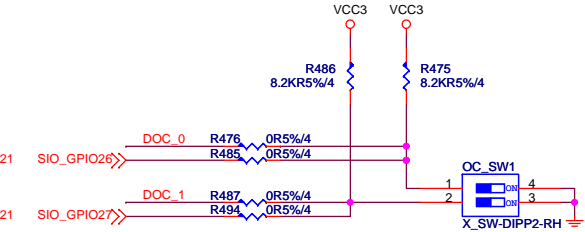
Pin16: 48MHz clock output. / 3.3V tolerant input  
for CPU frequency selection. Low voltage  
threshold inputs, see input electrical  
characteristics for Vil\_FS and Vih\_FS values.

Pin19: 14.318 MHz reference clock. / 3.3V  
tolerant input for CPU frequency selection.  
Refer to input electrical characteristics for  
Vil\_FS and Vih\_FS values.

OFF=1; ON=0

DOC	TABLE
1 0	CPU FREQUENCY
1 1	133 MHz ( default )
1 0	142 MHz
0 1	150 MHz
0 0	166 MHz

( Default ) OFF / OFF  
OFF / ON  
ON / OFF  
ON / ON

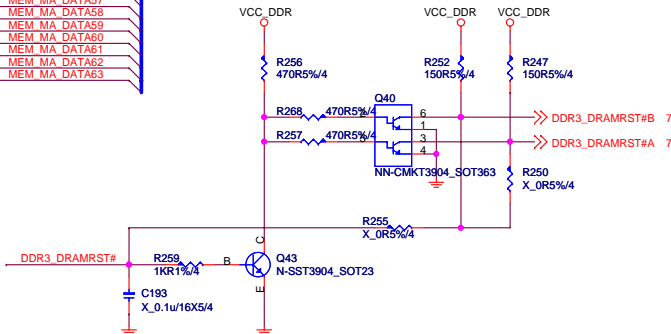
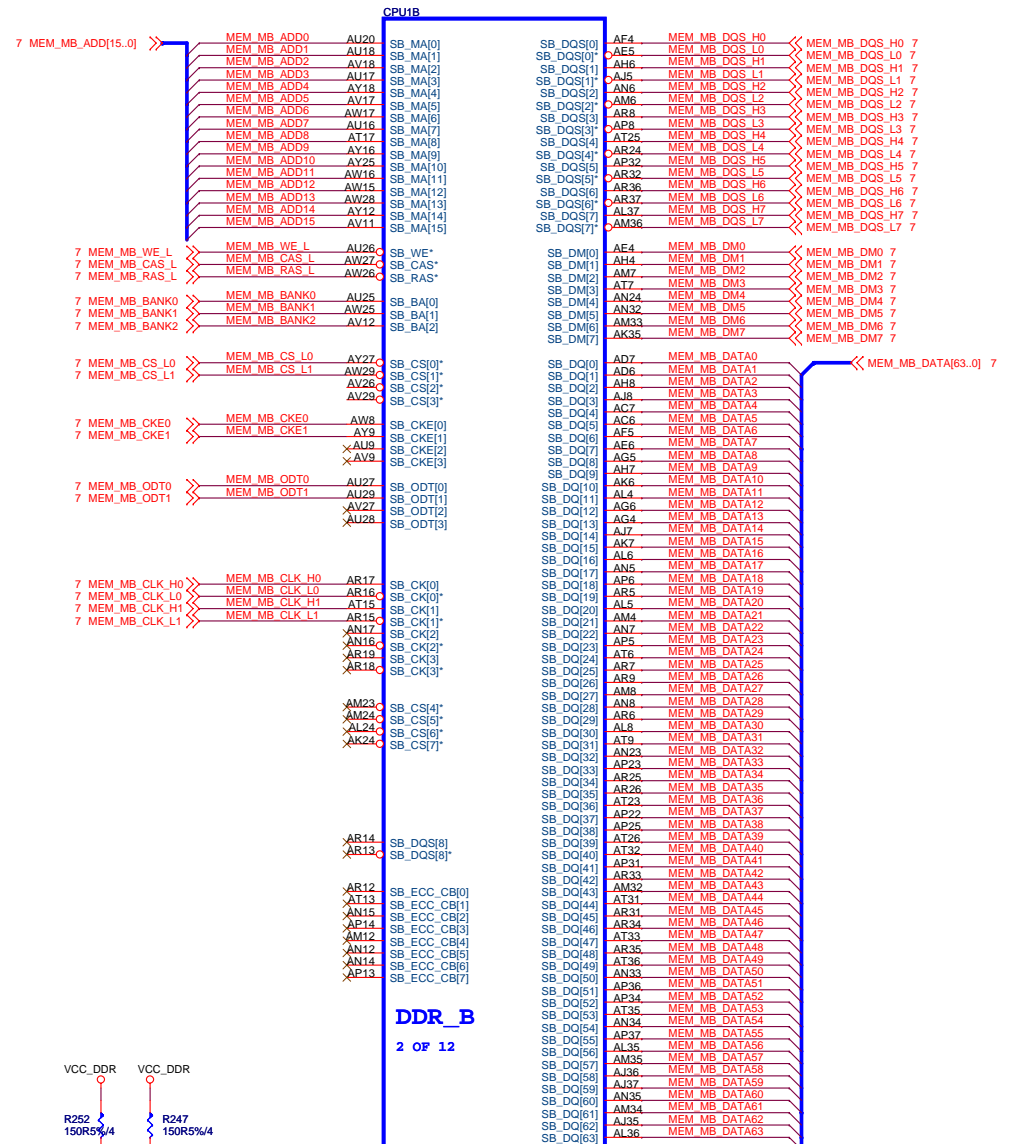
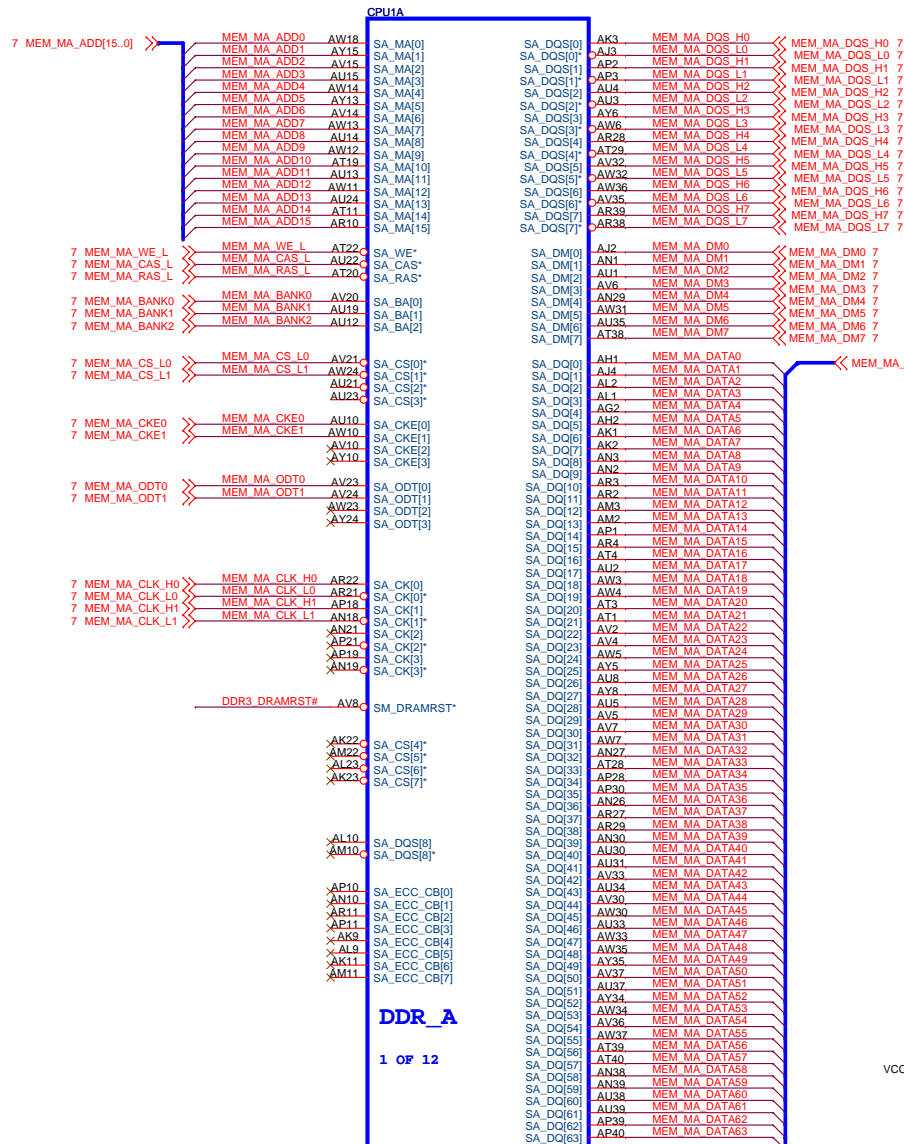


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**MS-7636**

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Custom	<b>CLK - ICS 9LRS4105B</b>	3.1

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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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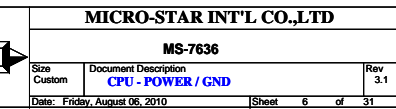
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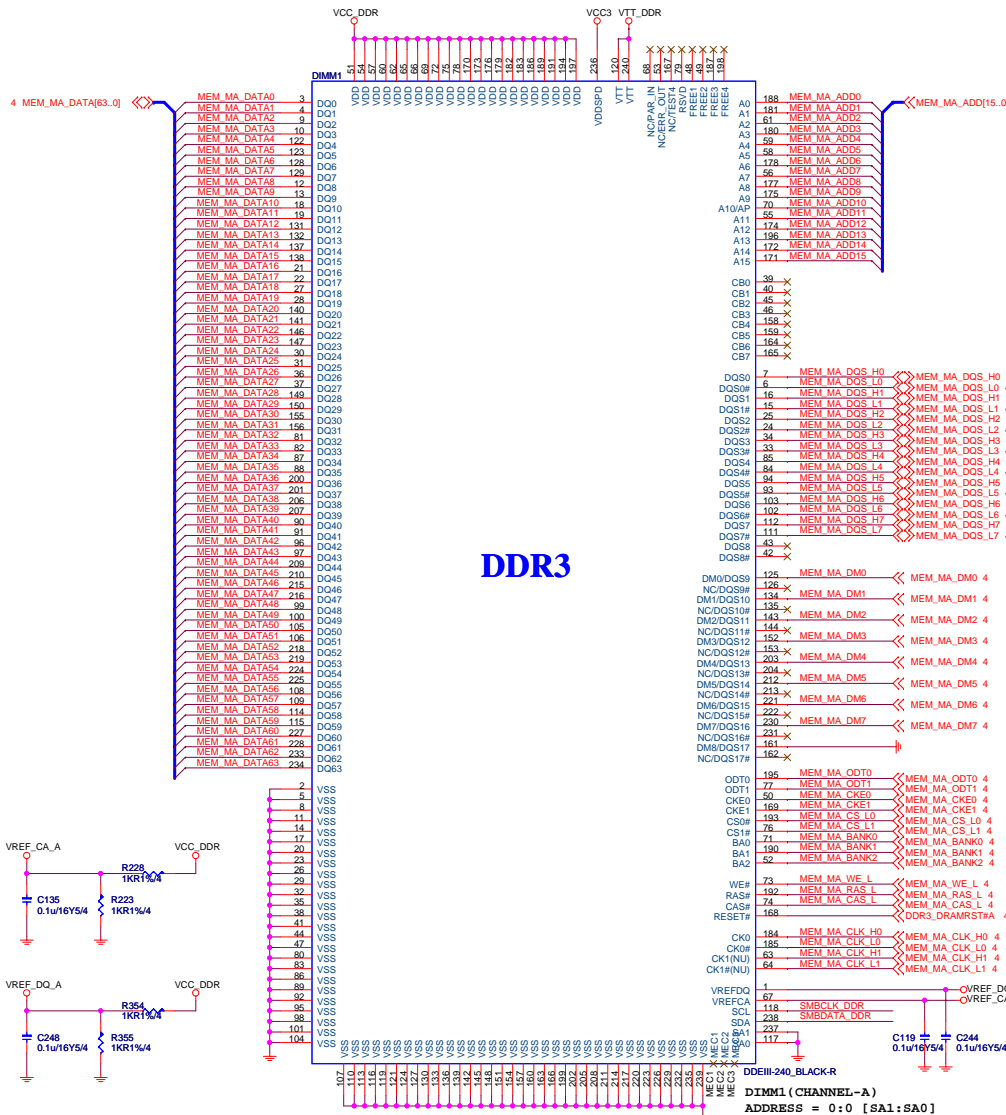
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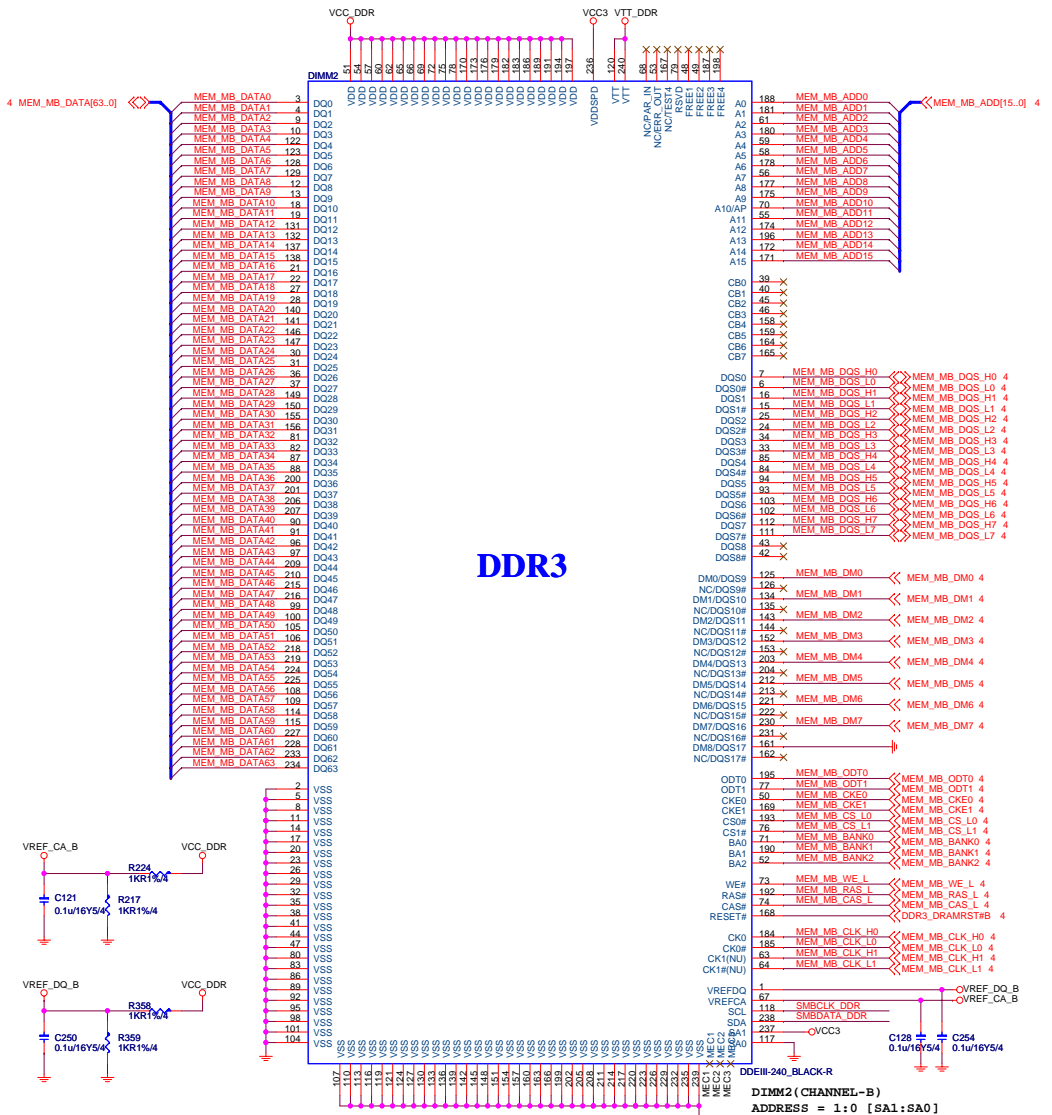


# DDR3 DIMM\_A0



DDR3

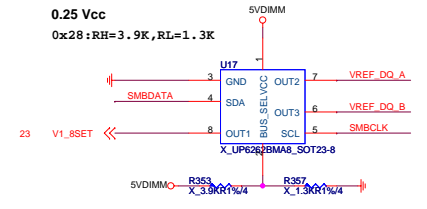
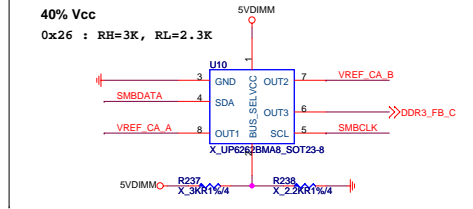
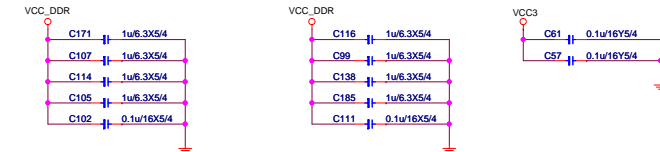
# DDR3 DIMM\_B0



DDR3

Place close to DIMM1

Place close to DIMM2



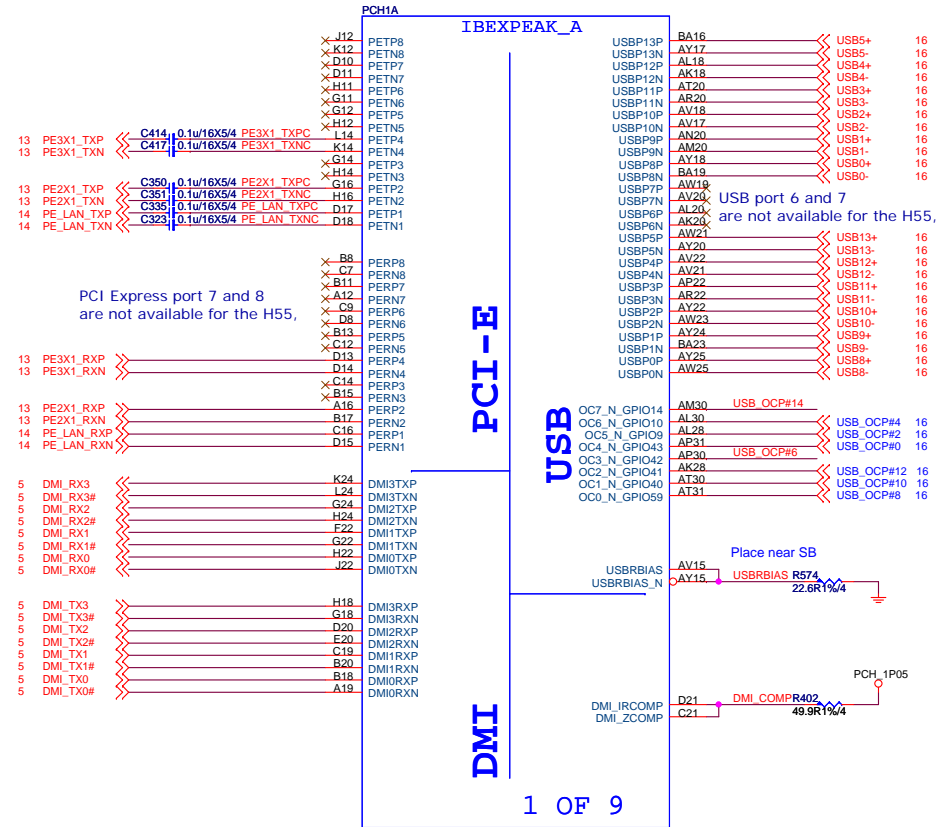
Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.3	3	3.9	open
BUS_SEL Voltage (% of VCC)	0	25	40	60	75	100

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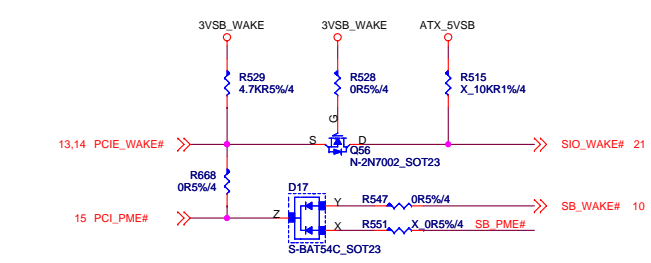
**MS-7636**

**DDR3 - DIMM1 / 2**

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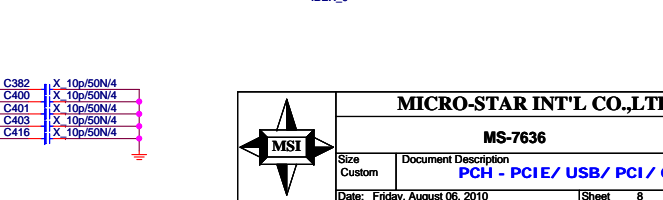
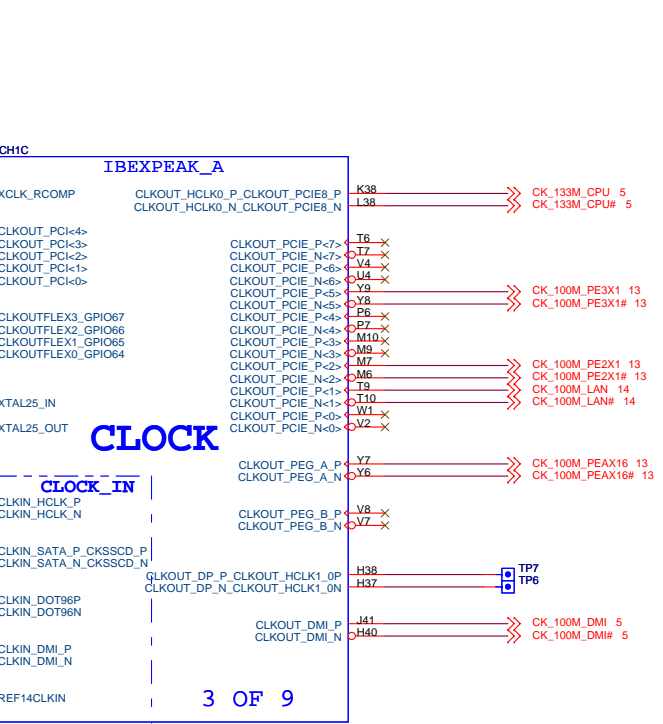
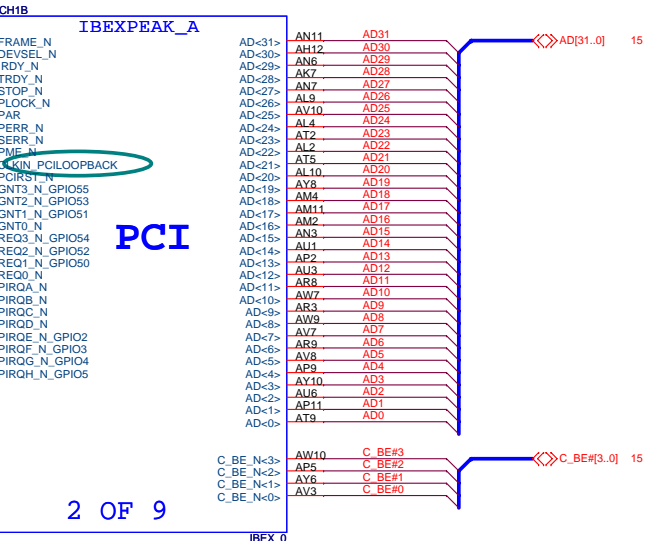
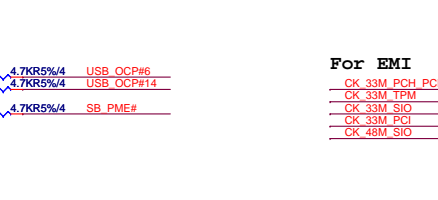
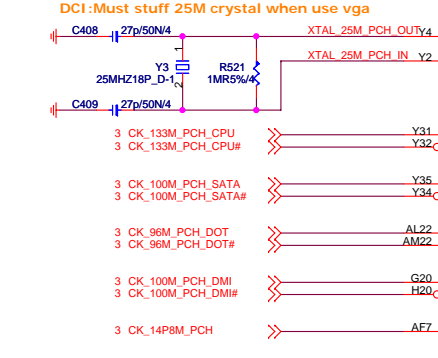
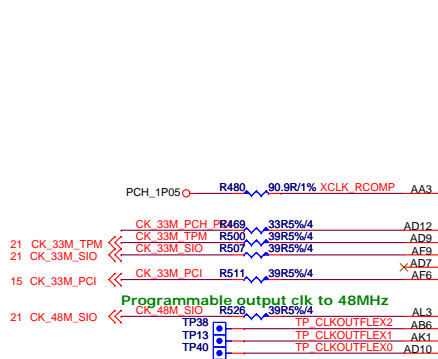
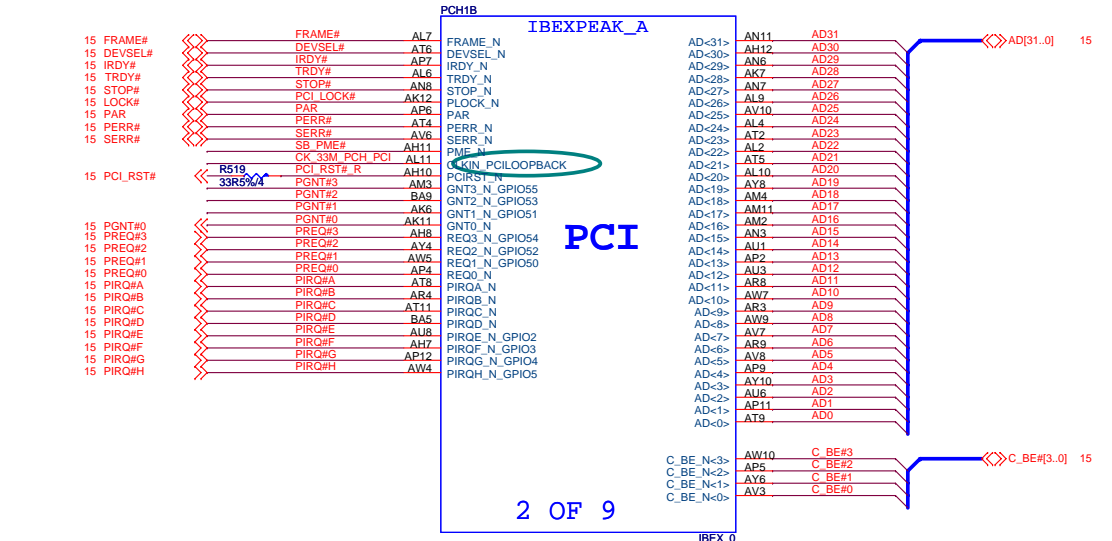


LAN WAKE UP CTRL



ROM Strap		
VCC3	R553 X 1KR5%/4	PGNT#0
	R520 X 1KR5%/4	PGNT#1
	R621 X 1KR5%/4	PGNT#0
	R522 X 1KR5%/4	PGNT#1
GNT#1	GNT#0	BOOT DEVICE
0	0	LPC
0	1	Reserved
0	1	PCI
1	1	SPI

Functional Strap		
Signal has a weak internal pull-High		
PGNT#2	R563 X 1KR5%/4	
PGNT#3	R531 X 4.7KR5%/4	
DMI for ESI compatible PGNT#2		
	HIGH	LOW
Top-Block Swap Mode PGNT#3	Effect	Override



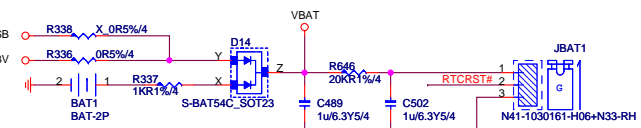
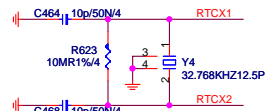
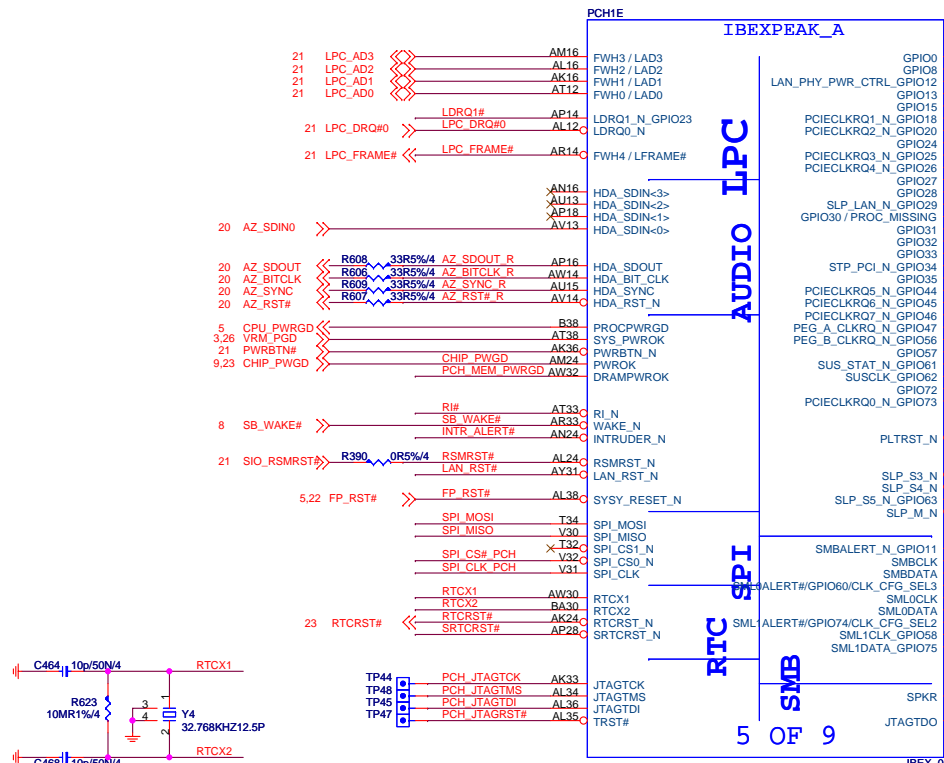
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Size	Document Description	Rev
Custom	<b>PCH - PCIE / USB / PCI / CLK</b>	3.1
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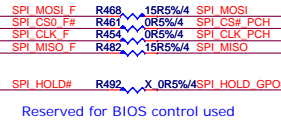
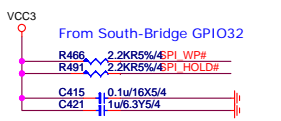






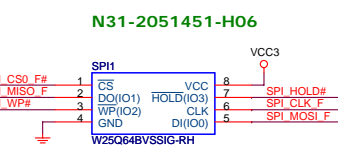
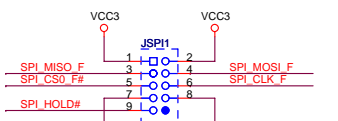
### SPI FLASH ROM

Place close to SB

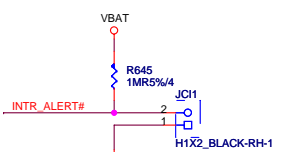


### SPI DEBUG PROT

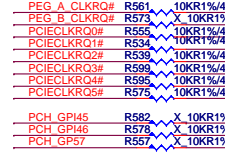
Close to SPI ROM



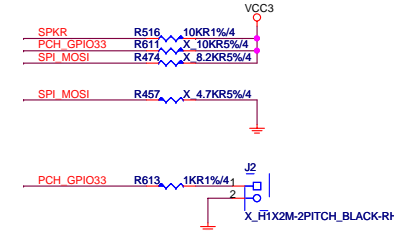
### Chassis Intrusion



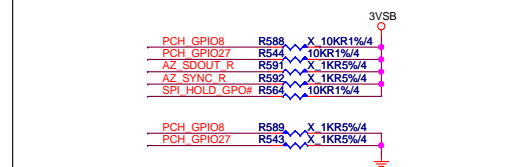
PEG\_A\_CLKREQ  
PCIECLKRQ1/2/4/5 must PD.



### Functional Straps

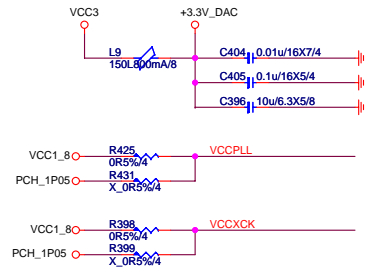
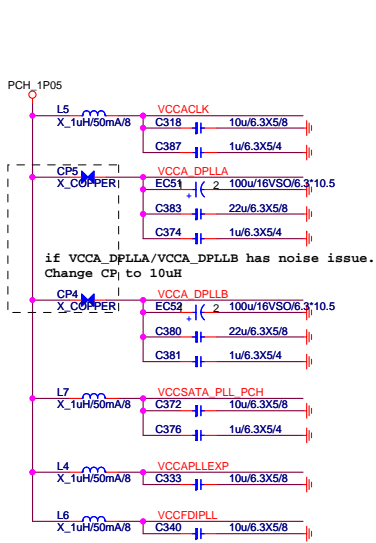


	HIGH	LOW
Flash Descriptor Security PCH_GPIO33 (internal pull-High)	Effect	Override
No Reboot Mode with TCO SPKR (internal pull-Low)	Enable	Disable
ITPM_ENB SPI_MOSI (internal pull-Low)	Enable ITPM	Disable ITPM



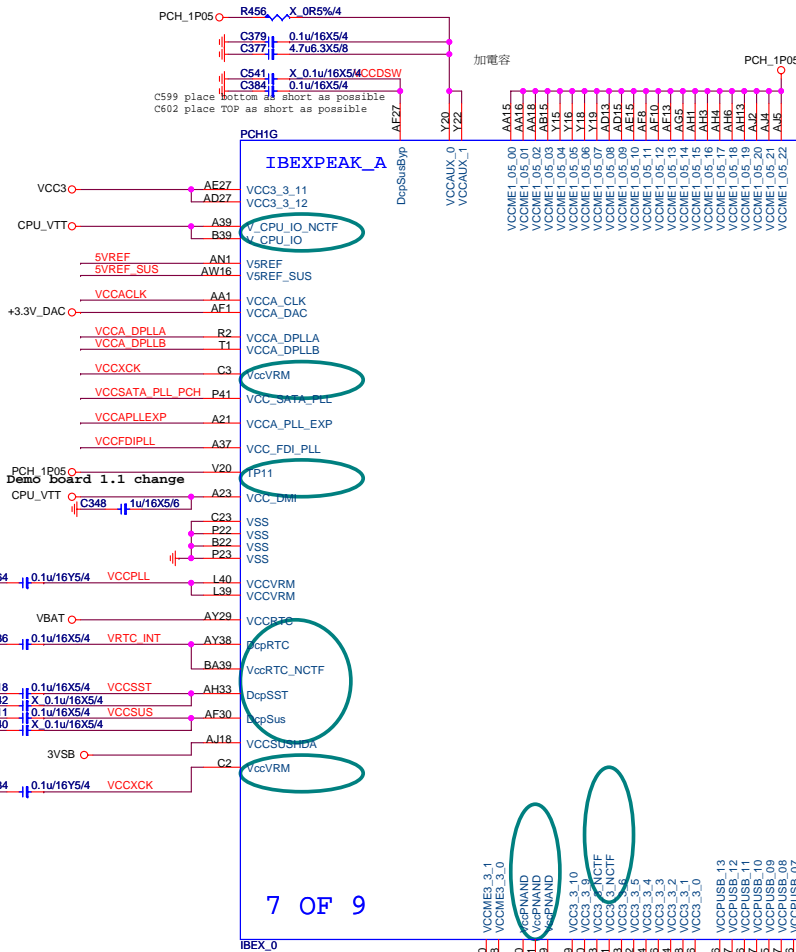
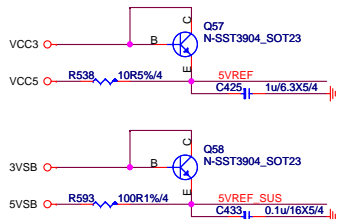
	HIGH	LOW
Integrated clock chip PCH_GPIO8 (internal pull-High)	Disable	Enable
OD PLL VR PCH_GPIO27 (internal pull-High)	Enable	Disable
NAND VCCQ PWR WELL HDA_SDO (internal pull-Low)	EPW	Powered By Core
OD PLL VR SUPPLY SEL HDA_SYNC (internal pull-Low)	1.5V SUPPLY	1.8V SUPPLY
TLS Confidentiality SPI_HOLD_GPO# (internal pull-Low)	Enable	Disable

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## 5VREF & 5VREF\_SUS Sequencing Circuit

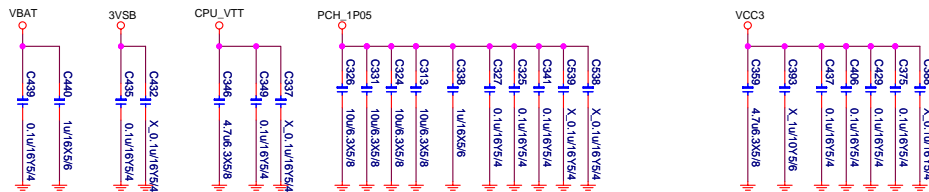
5VREF must be powered up before VCC3 or after VCC3 within 0.7V.  
Also, 5VREF must power down after VCC3 or before VCC3 within 0.7V.  
This rule is also applies to 5VREF\_SUS and 3VSB.  
However, the 3VSB is derived from the 5VSB on the power supply  
thru a voltage regulator and therefore, they can satisfy the requirement.



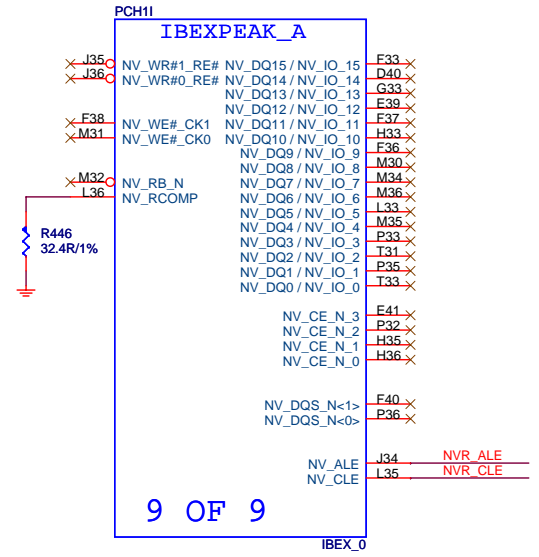
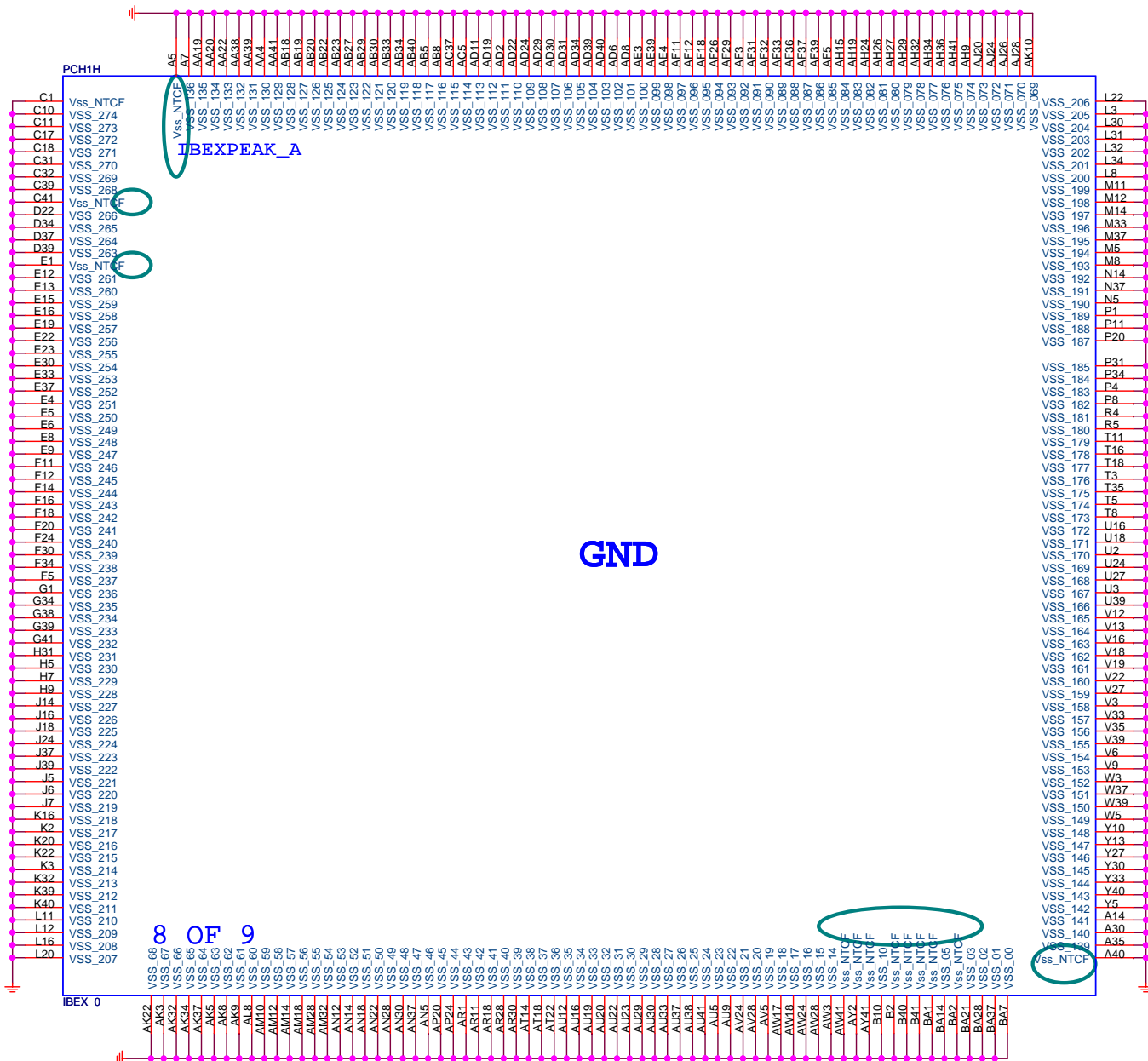
POWER

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## PCH decoupling cap



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Signal has a weak internal pull-low

VCC3

NVR\_CLE R438 X 10KR1%/4

NVR\_ALE R427 X 8.2KR5%/4

NVR\_ALE R426 X 4.7KR5%/4

	HIGH	LOW
DMI/ FDI Termination Voltage NVR_CLE	DC COUPLED: TX/RX TO VCC	DC COUPLED: TX/RX TO VSS
Danbury (Anti-Theft) TECH. NV_ALE	Enable	DISABLE

**MICRO-STAR INT'L CO.,LTD**

**MS-7636**

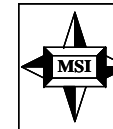
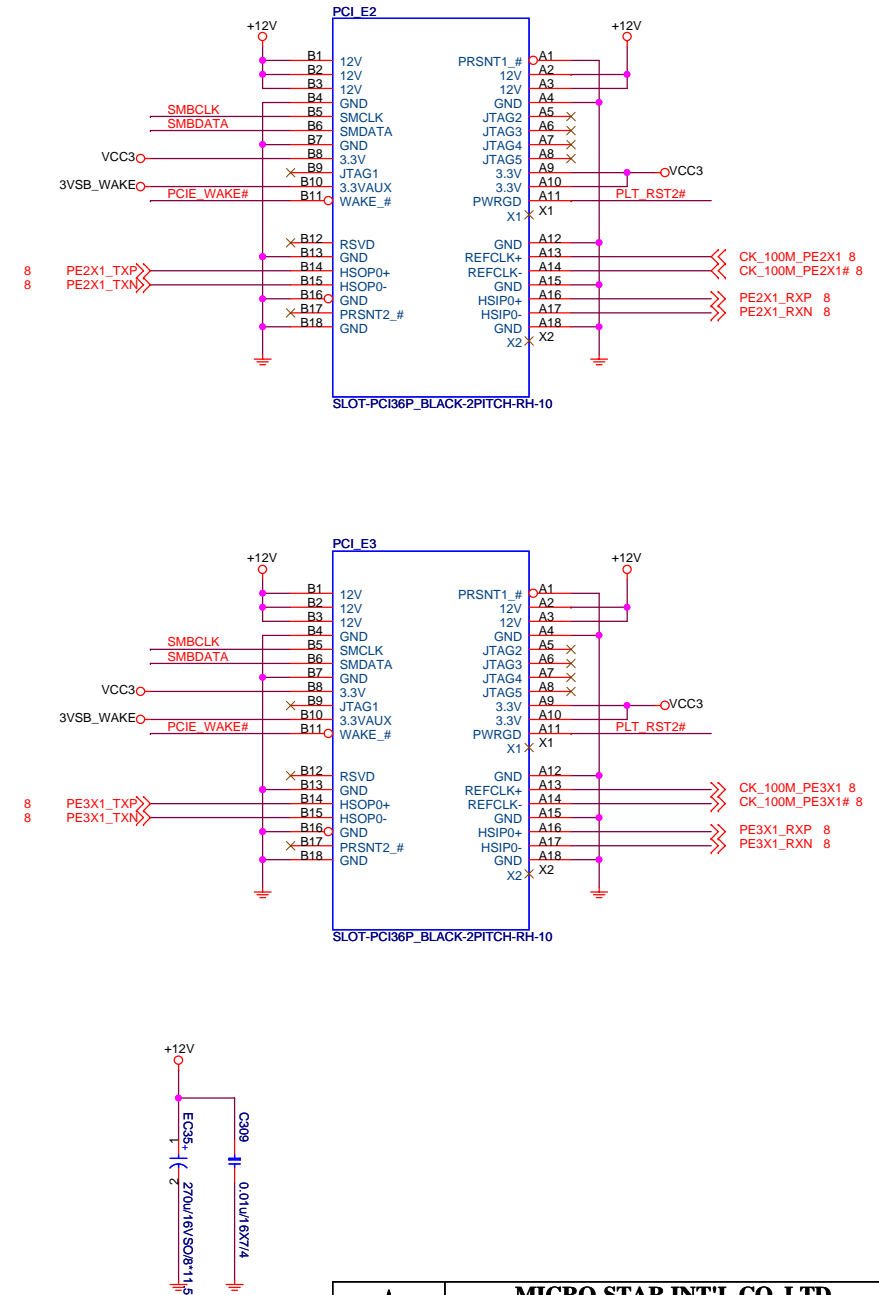
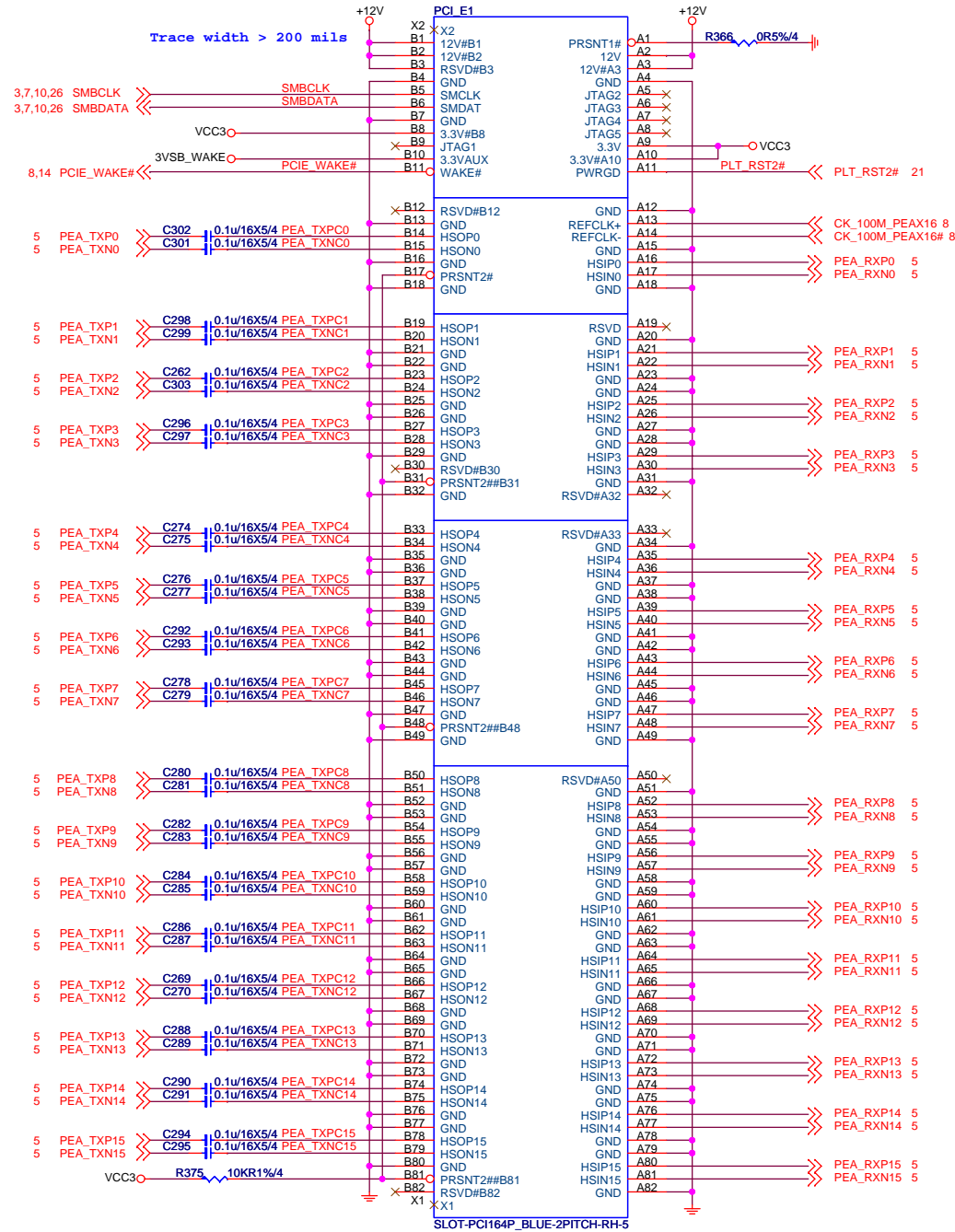
Size	Document Description	Rev
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# PCI\_Express X16 Slot

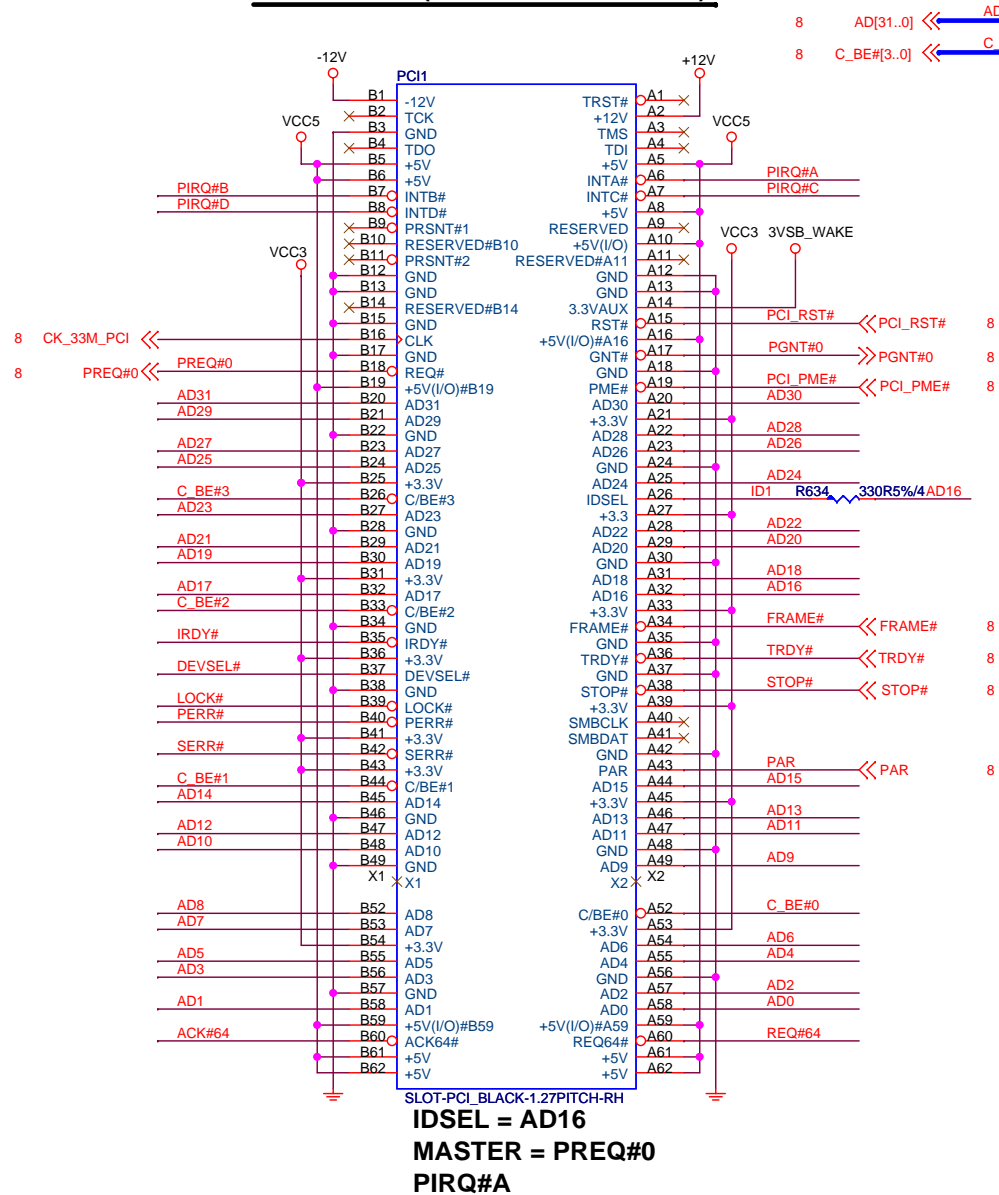
# PCI\_Express X1 Slot



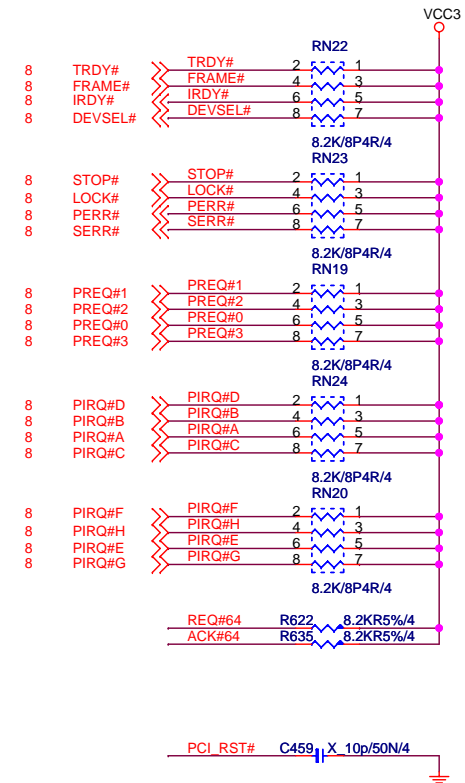
MICRO-STAR INT'L CO.,LTD		
MS-7636		
Size Custom	Document Description <b>PCI E SLOT - X16 / X1</b>	Rev 3.1
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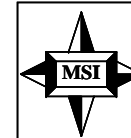
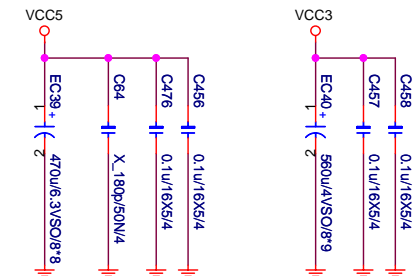
## PCI SLOT 1 (PCI VER: 2.2 COMPLY)



## PCI PULL-UP / DOWN RESISTORS



## PCI SLOT DECOUPLING CAP

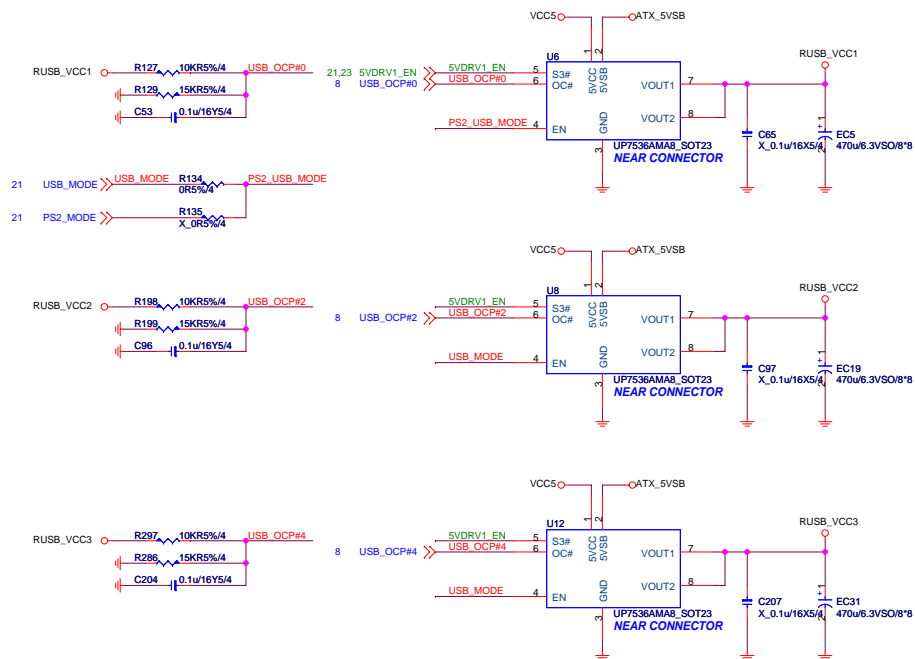


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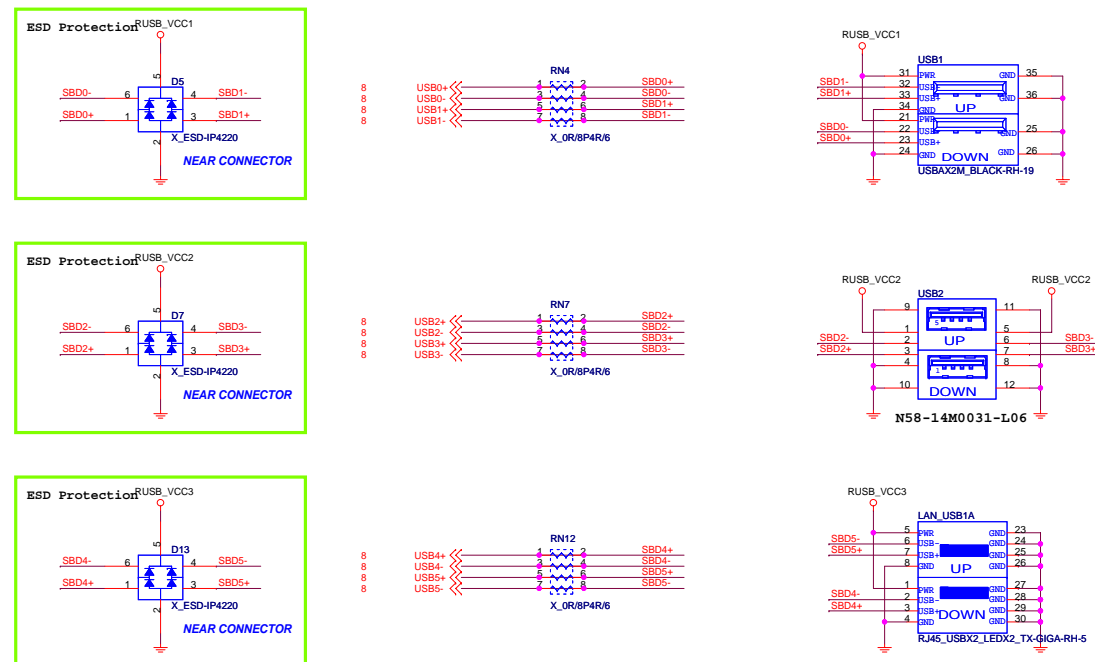
MS-7636

Size	Document Description	Rev
Custom	PCI SLOT	3.1
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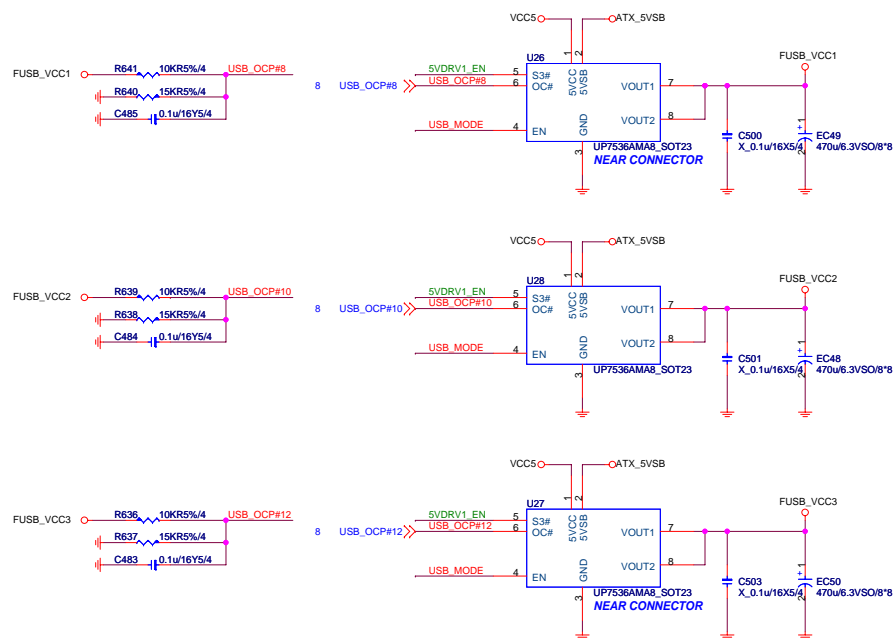
## POWER CIRCUIT FOR USB PORT 0 ~ 5



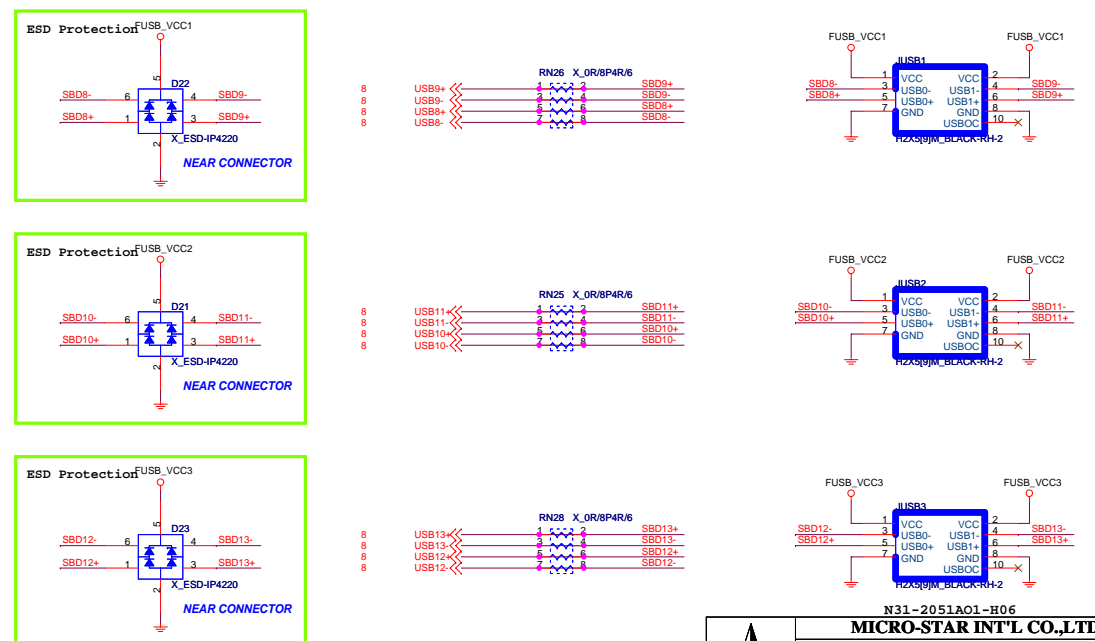
## REAR PANEL USB CONNECTOR FOR USB PORT 0 ~ 5



## POWER CIRCUIT FOR USB PORT 6 - 11



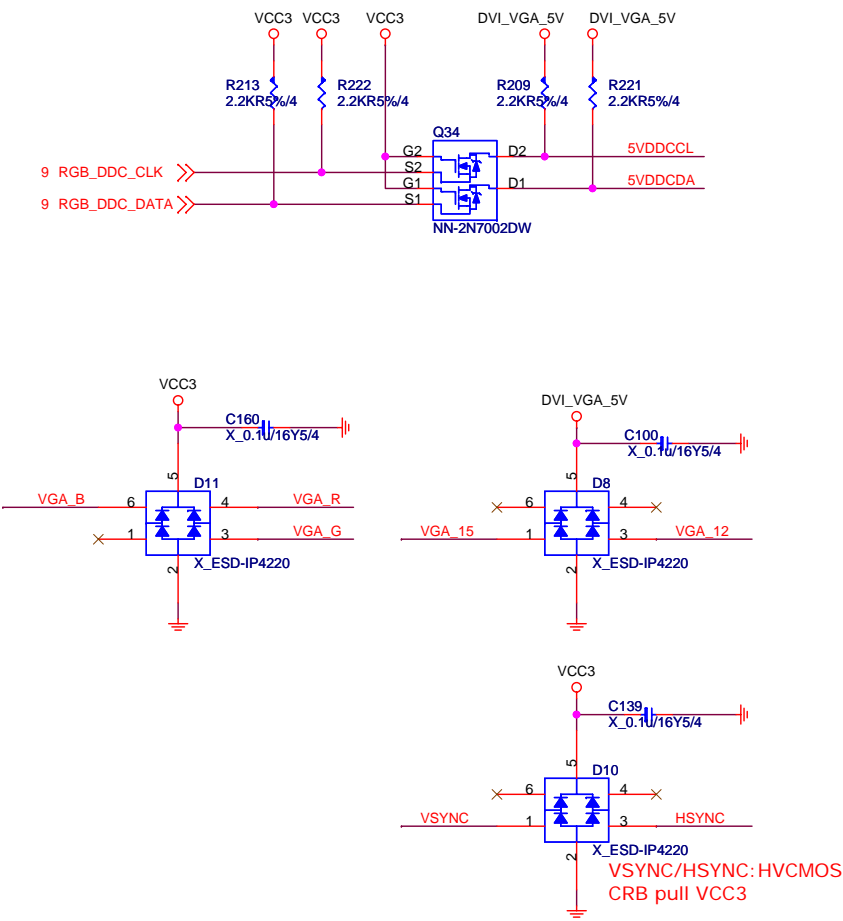
## FRONT PANEL USB CONNECTOR FOR USB PORT 6 ~ 11



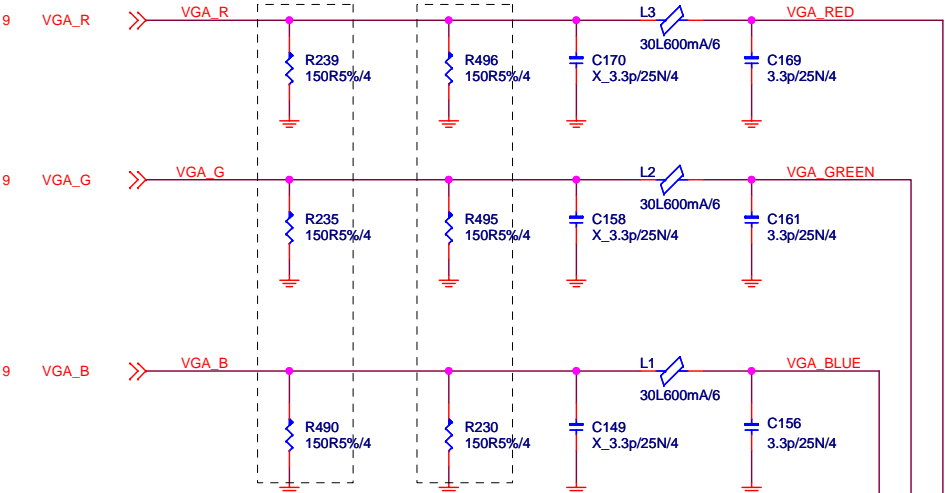


D-Sub

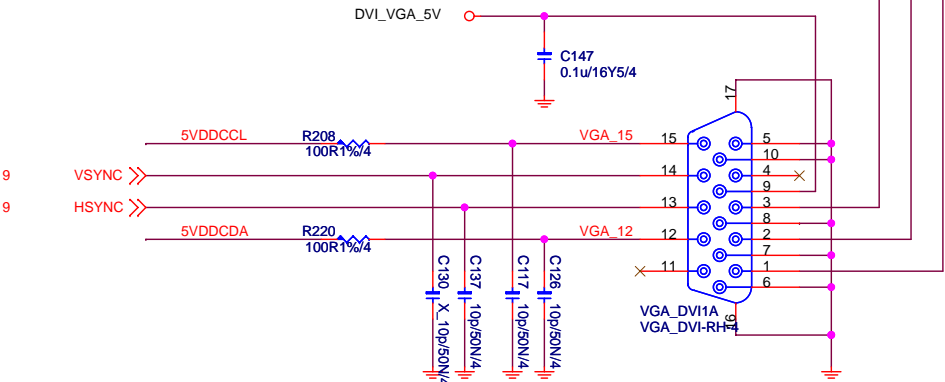
Level shift



PLACE CLOSE TO VGA CONNECTOR,  
WITHIN 750 MIL OF PIN



Close to PCH within 250 mils.



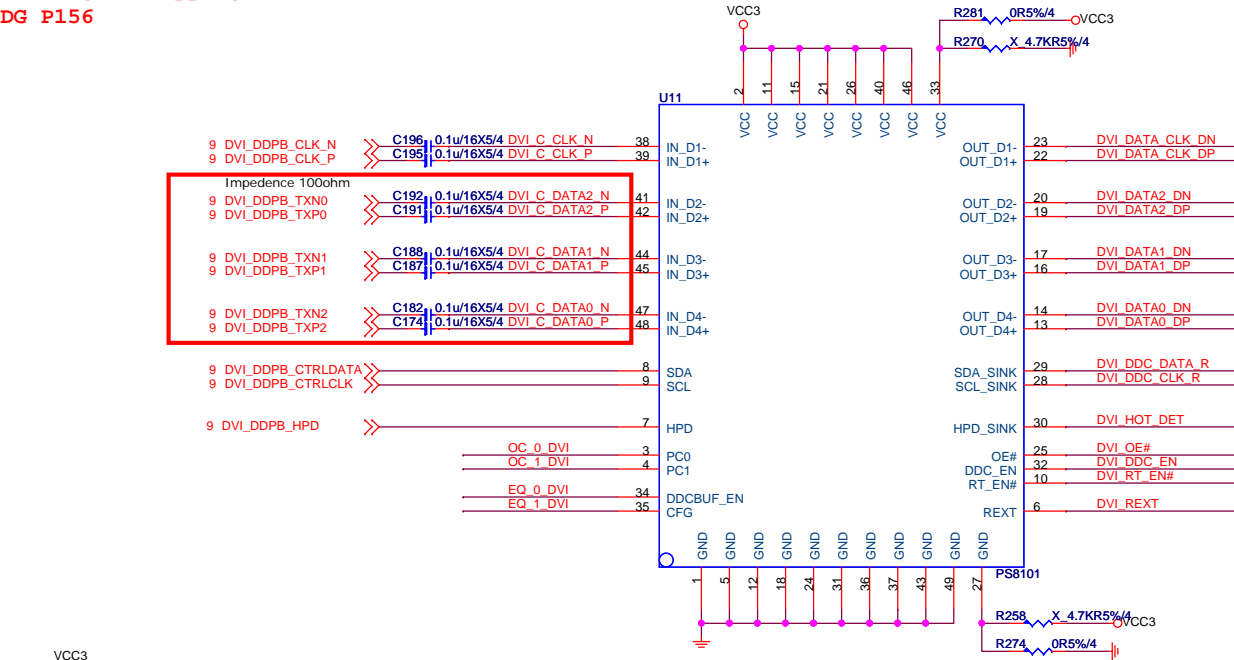
MICRO-STAR INT'L CO.,LTD

MS-7636

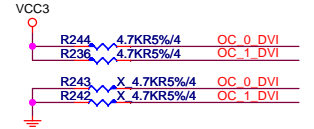
Size Custom	Document Description VGA	Rev 3.1
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DVI level shifter

PCH signal Mappings  
DG P156

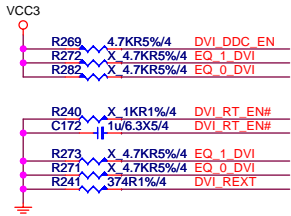


PARADE料號: B0B-081010C-P97

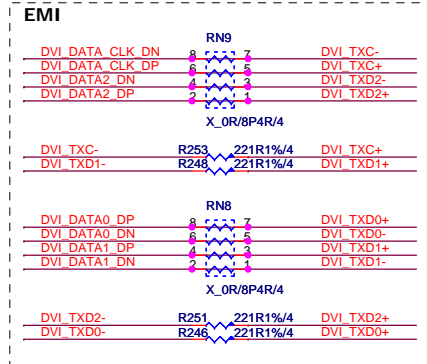
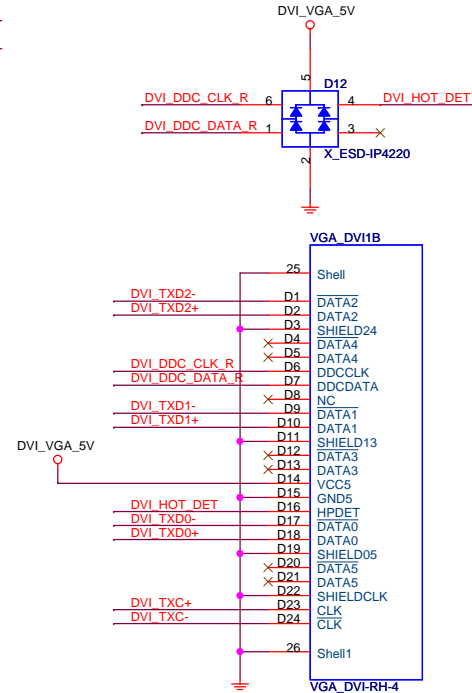
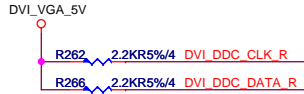
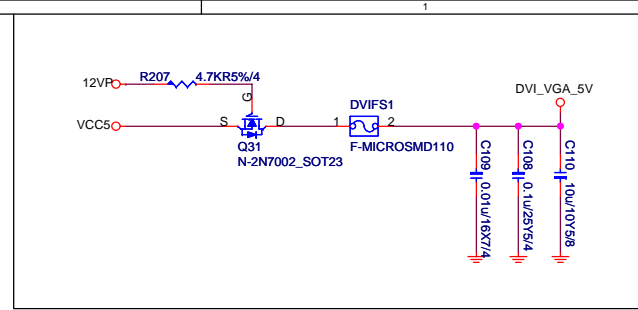
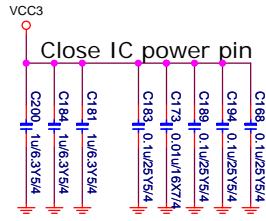
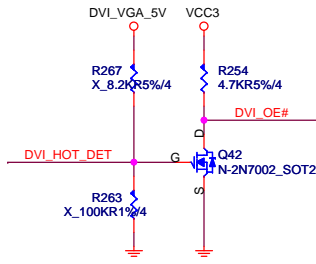


PC1	PC0	
0	0	8 dB
0	1	4 dB
1	0	12 dB
1	1	0 dB

DDC_EN, DDCBUF_EN, OE#	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off



	0	1	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	Internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination resistors are set to high impedances the chip is power down and input termination resistors will be at high impedance.	Internal pull-down at ~500K ohm.
OE#	Enable	Disable	Internal pull-down at ~500K ohm.
HPD_SINK	Disable	Enable	Internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		Internal pull-down at ~500K ohm.
REXT			analog current generation.



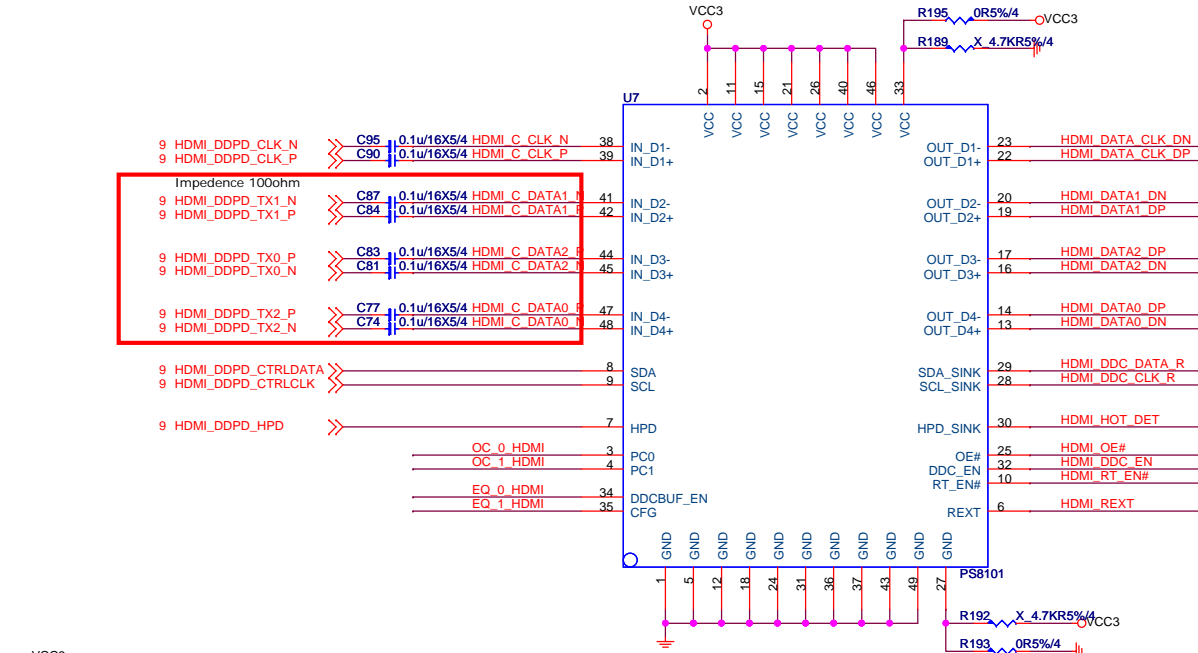
**MICRO-STAR INT'L CO.,LTD**

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HDMI level shifter



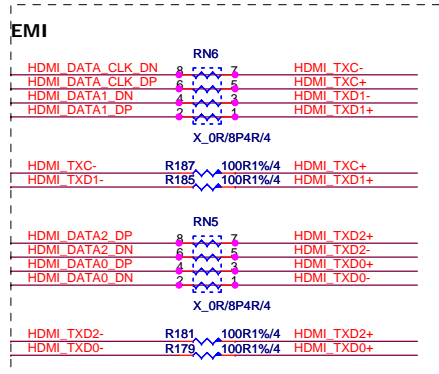
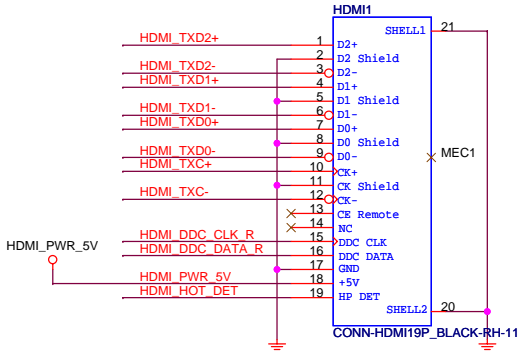
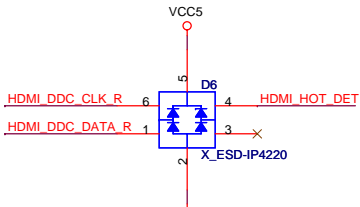
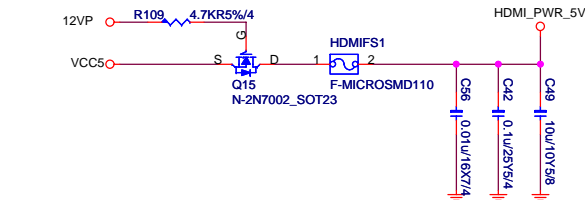
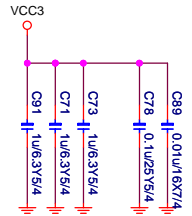
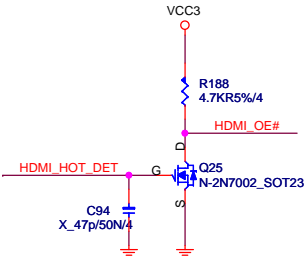
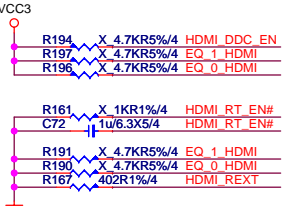
VCC3

R163 4.7KR5%/4 OC 0 HDMI  
R162 4.7KR5%/4 OC 1 HDMI  
R169 X 4.7KR5%/4 OC 0 HDMI  
R168 X 4.7KR5%/4 OC 1 HDMI

PC1	PC0	
0	0	8 dB
0	1	4 dB
1	0	12 dB
1	1	0 dB

DDC_EN, DDCBUF_EN, OE#	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

	0	1	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	Internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination resistors are set to high impedances the chip is power down and input termination resistors will be at high impedance.	Internal pull-down at ~500K ohm.
OE#	Enable	Enable	Internal pull-down at ~500K ohm.
HPD_SINK	Disable	Enable	Internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		Internal pull-down at ~500K ohm.
REXT			analog current generation.



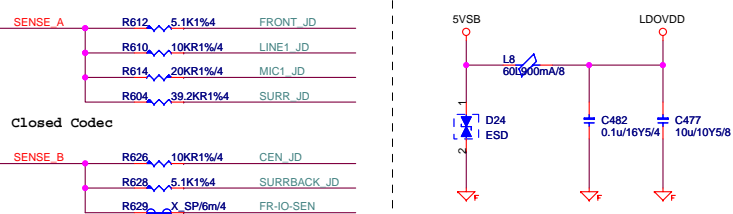
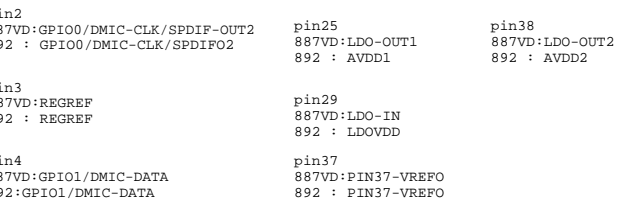
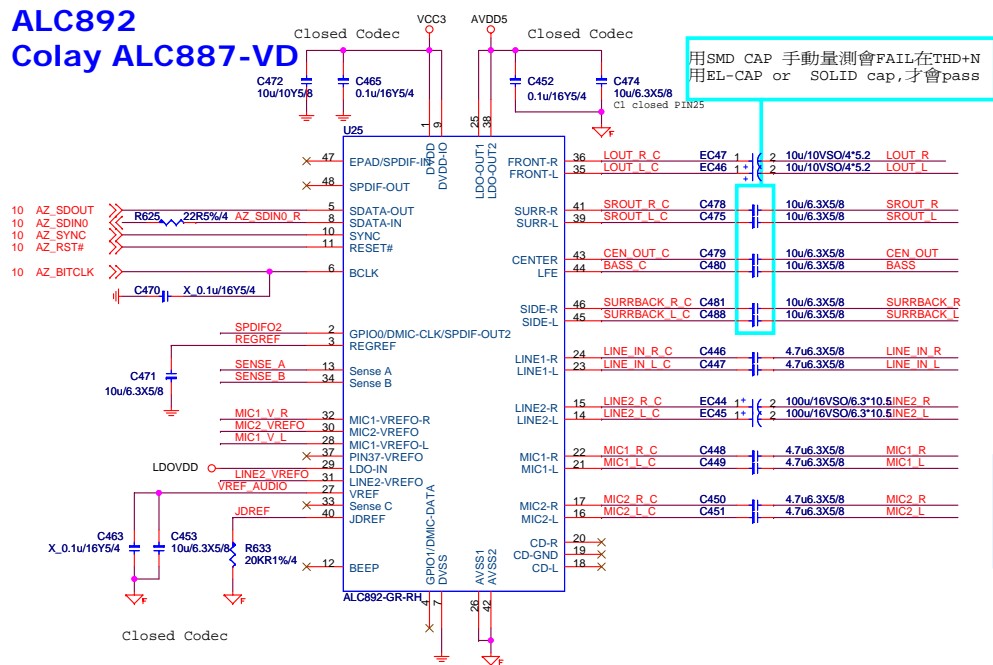
**MICRO-STAR INT'L CO.,LTD**

**MS-7636**

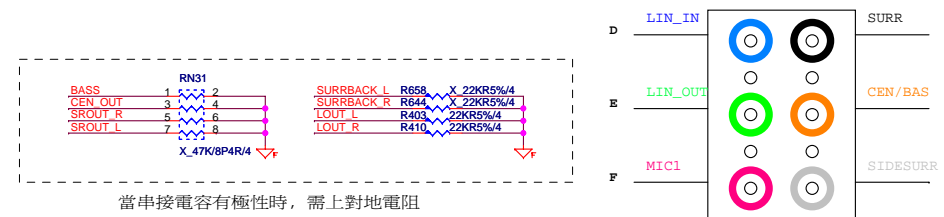
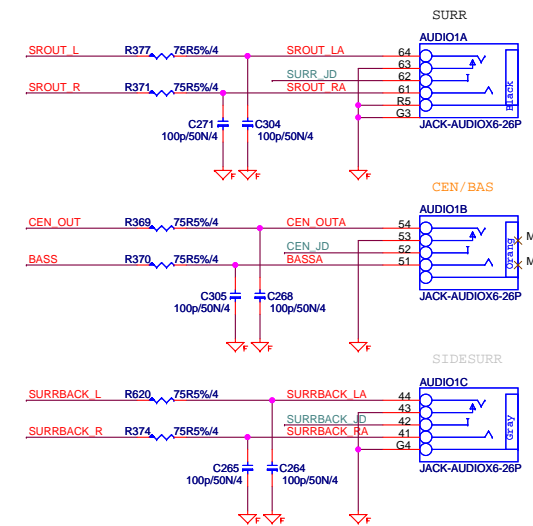
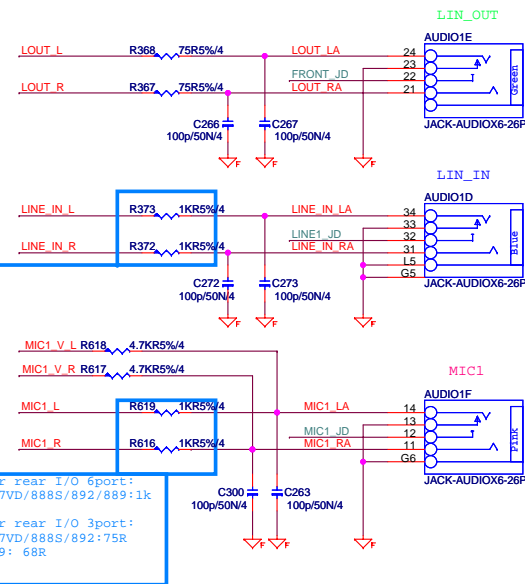
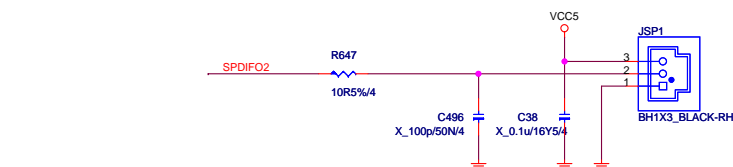
Size Custom Document Description **HDMI - PARADE PS8101** Rev 3.1

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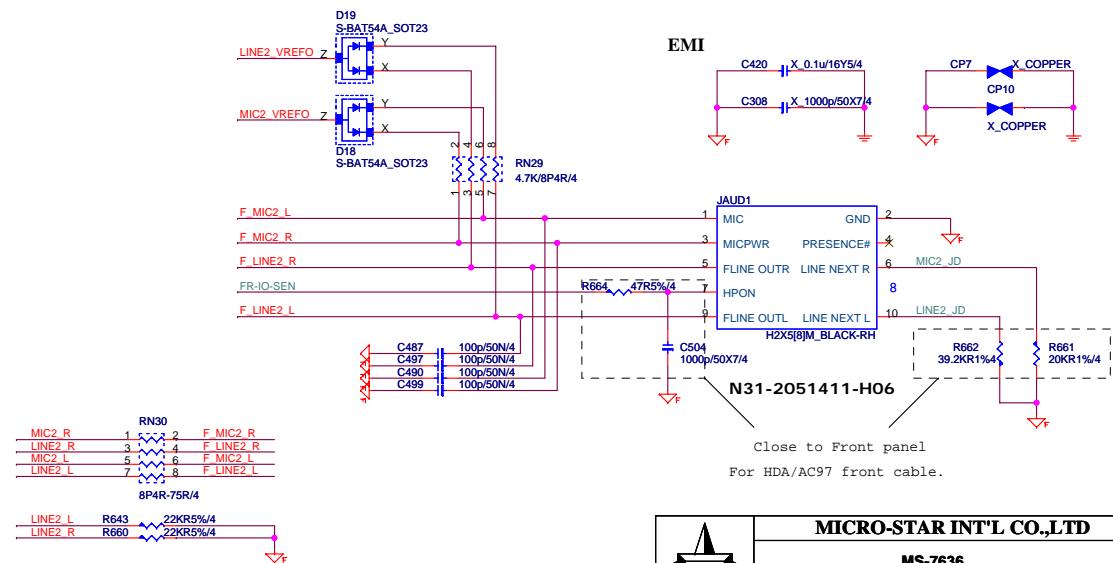
ALC892  
Colay ALC887-VD



PDIF OUT

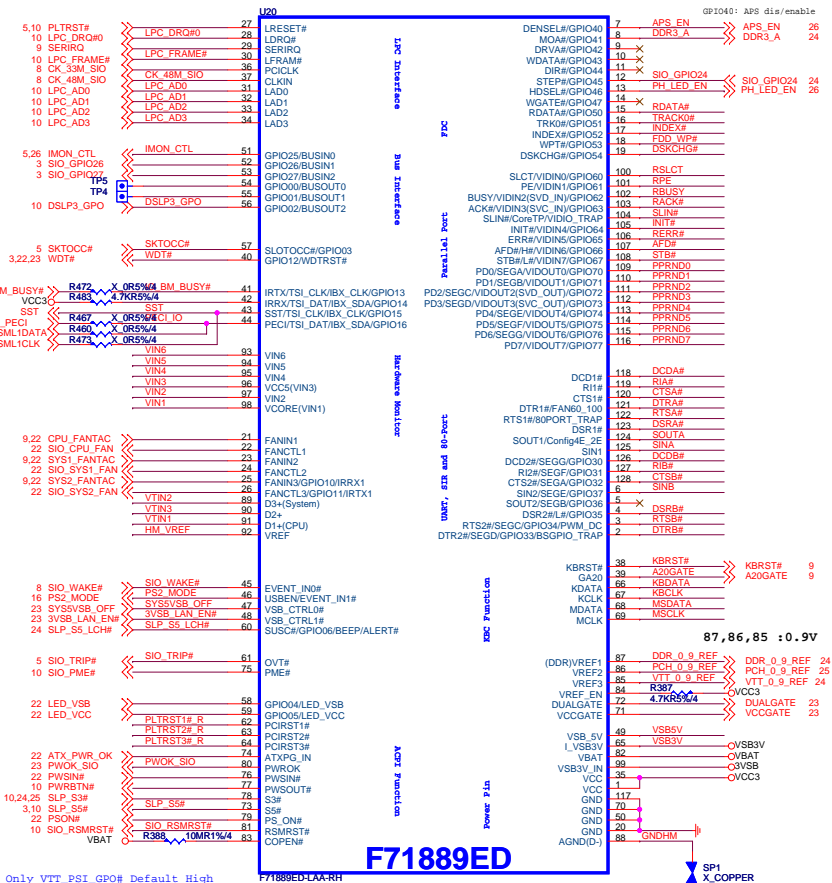


當串接電容有極性時，需上對地電阻

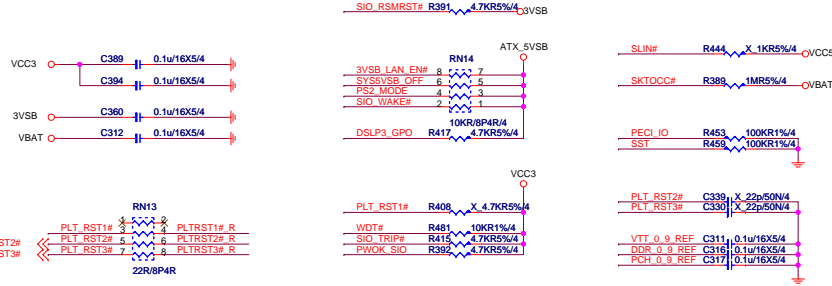


<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7636</b>			
Size Custom	Document Description <b>Audio Codec - ALC889/ ALC 887</b>		Rev 3.1
Date: Friday, August 06, 2010		Sheet 20 of 31	



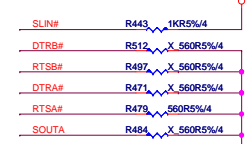


Only VTT\_PSI\_GPO# Default High  
Others Default Low

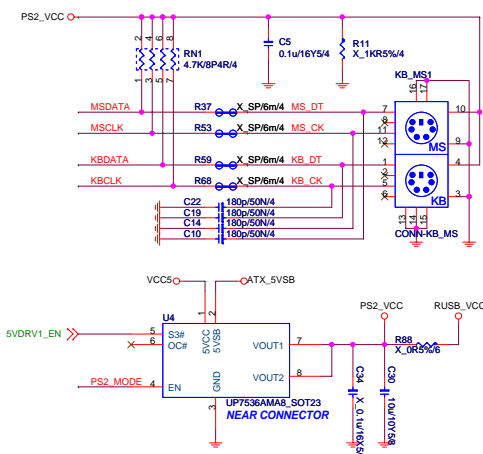


### Strapping RESISTOR & Others Pull Hi Resistor

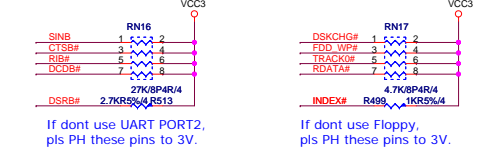
Don't STUFF	STUFF
SLIN#	Pull high 1k Pin 100-116 as LPT interfaces
DTRB#	PIN 51-56 = GPO
RTSB#	PIN 51-56 = BUS
PWM_FAN	LINEAR FAN
DTRA#	FAN START DUTY 60%
RTSA#	FAN START DUTY 100%
SOUTA	80 PORT ENABLE
	80 PORT DISABLE
	CONFIG 4E
	CONFIG 2E



### PS2 KEYBOARD & MOUSE CONNECTOR



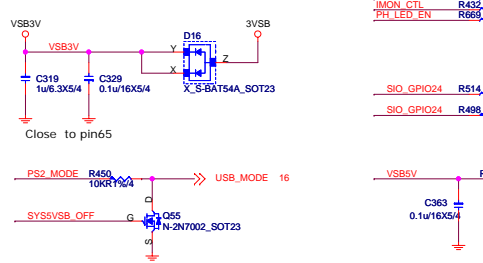
### COM2 / FLOPPY BOBCK



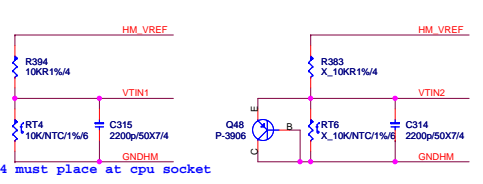
### JLPC port for TPM



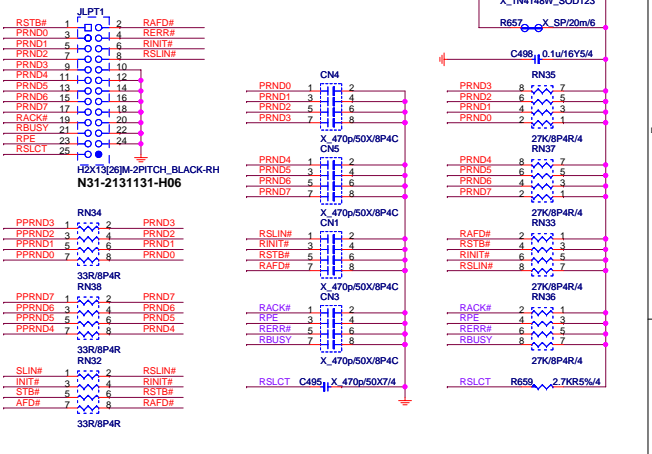
### Eup CTL BLOCK



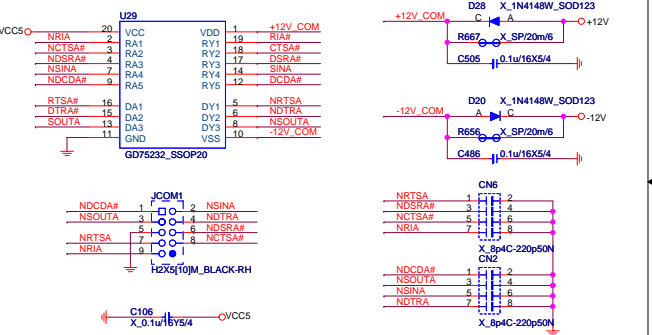
### Temperature Sensing



### PARALLEL PORT

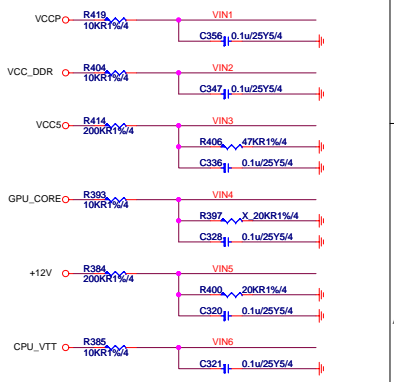


### SERIAL PORT (COM 1)



### VOLTAGE SENSING(H/W Monitor)

The best voltage input level is about 1V.

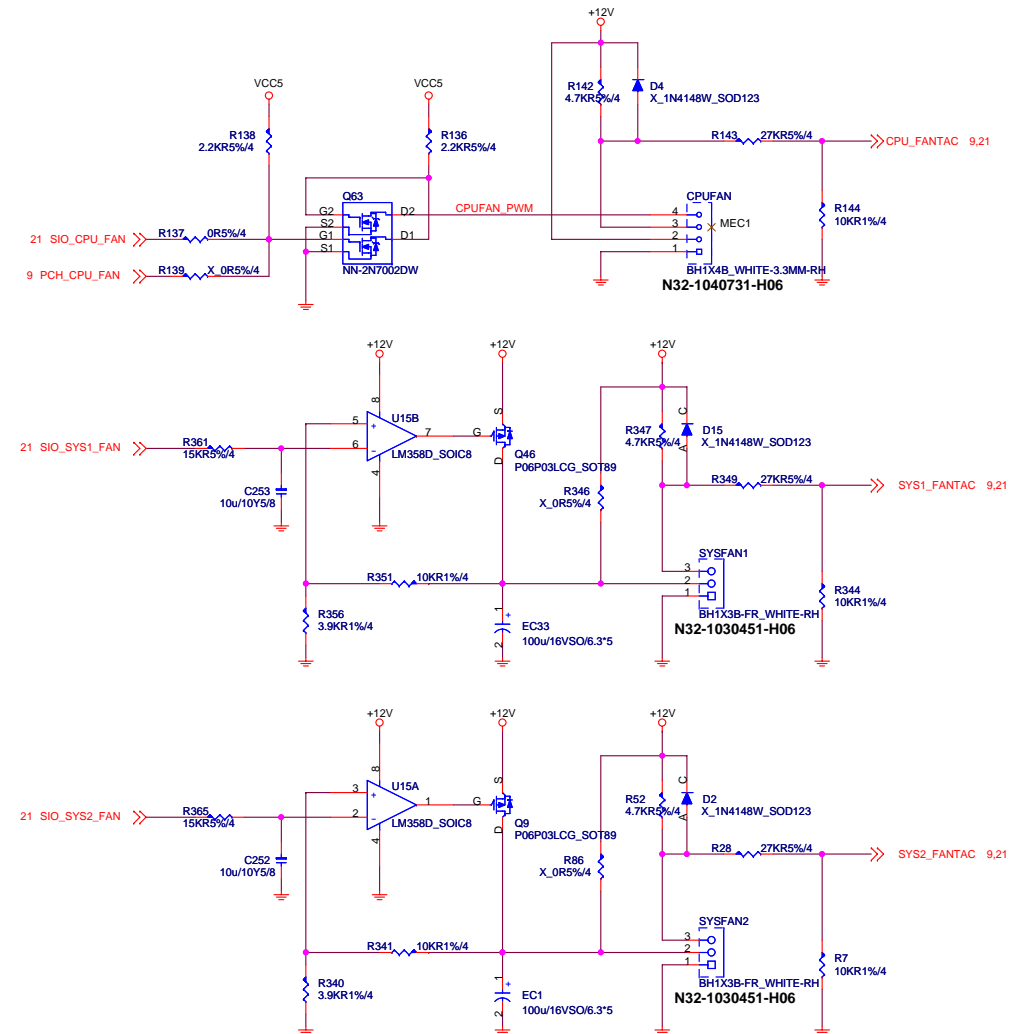
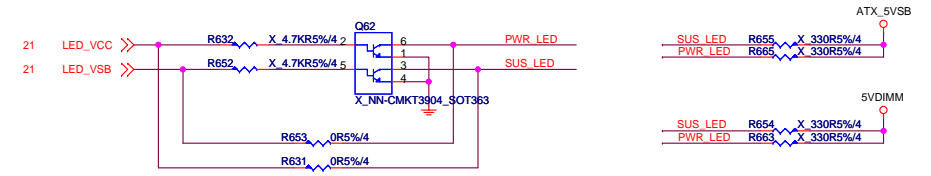
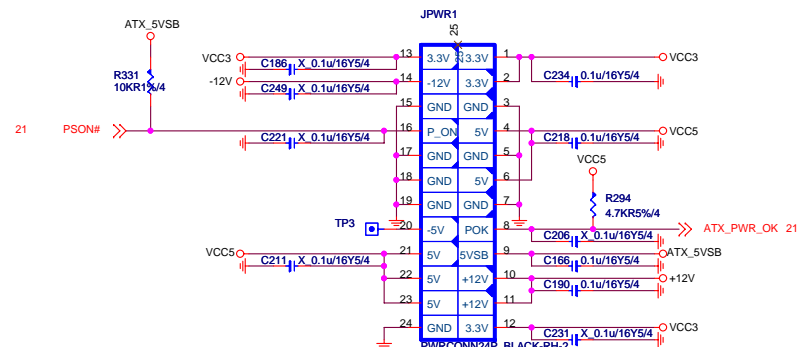


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Size Custom Document Description SIO - F7889ED/ COM/ LPT/ TPM Rev 3.1

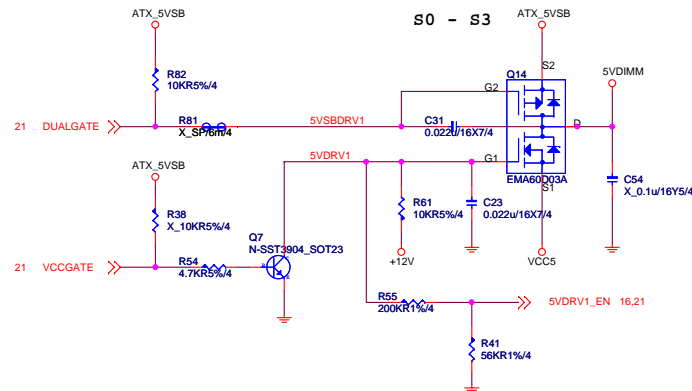
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## 5VDIMM

S0 - S3

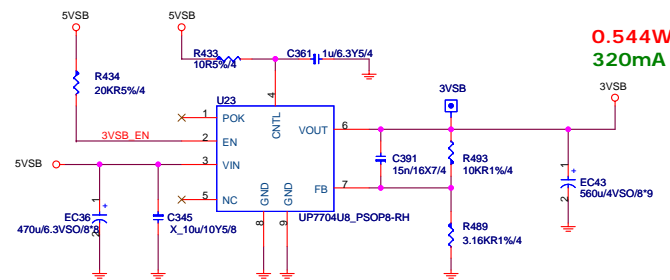
For DDR, 6.581A



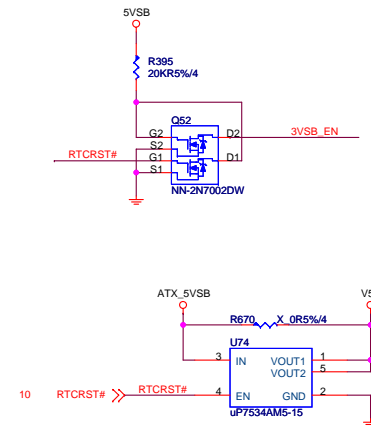
## 3VSB

S0 - S5

For PCH, 320mA



0.544W  
320mA

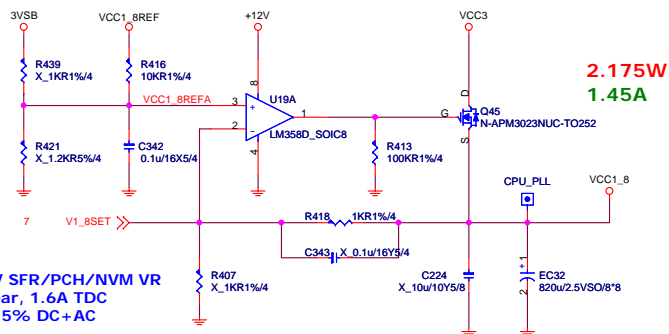


## VCC1\_8

S0

For CPU SFR, 1.35A

For PCH PLL, 0.1A



2.175W  
1.45A

1.8V SFR/PCH/NVM VR  
Linear, 1.6A TDC  
+/- 5% DC+AC

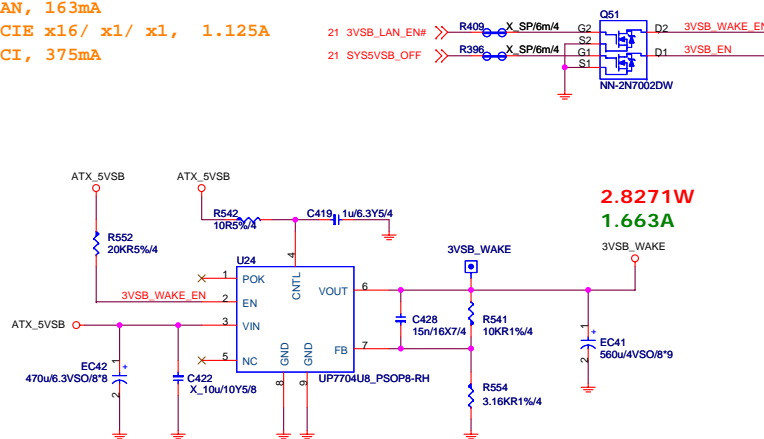
## 3VSB\_WAKE

S0 - S5

For LAN, 163mA

For PCIE x16/ x1/ x1, 1.125A

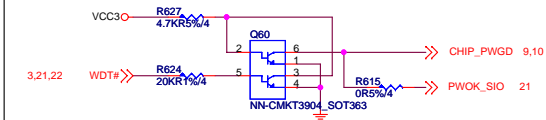
For PCI, 375mA



2.8271W  
1.663A

## PWROK DELAY

VID before PWROK > 3ms

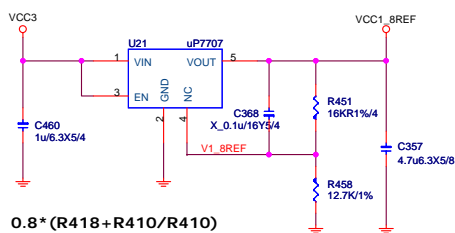


## cpvtt & pch vore wait 1.8v



## VCC1\_8REF

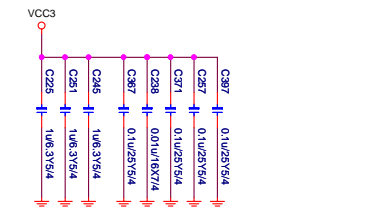
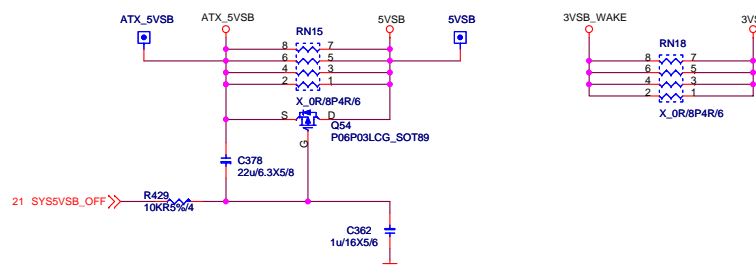
S0



0.8\* (R418+R410/R410)

## 5VSB Power Switch

Trace Width 80mils.



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Custom	ACPI controller UPI	3.1
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S0 - S3

The schematic diagram illustrates a power supply circuit for a system board. Key components include:

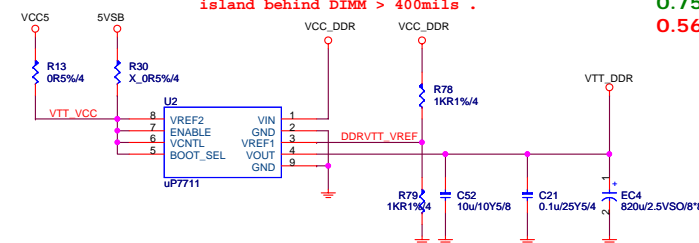
- D9 S-BAT54C\_SOT23**: A diode connected between +12V and 5VDIMM.
- U8 FB**: A feedback component connected to Vref, VCC, BOOT, PHASE, UG, LG, and GND.
- U9 CH-1.2u15A1.7m**: A choke connected to 5VDIMM\_IN and 5VDIMM.
- U10 CH-1.2u27A1.7m**: A choke connected to VDD\_DDR and VCC\_DDR.
- U11 DRAM**: A memory module connected to VCC\_DDR.
- U12 Q36 NN-CMKT3604\_SOT363**: A MOSFET connected to ATX\_5VSB, DDR\_REF, and SLP signals.

Other components shown are various resistors (R211, R215, R210, R218, R226, R227, R225, R206, R182) and capacitors (C113, C122, C127, C128, C29, C28, C23, C22, C157). The circuit also includes a 5VDIMM input and a 5VSB output.

19.5A  
29.25W

## VTT DDR:0.75A

0.75A  
0.562W



Only for meet Intel power down sequence.

SO

H:1.05  
L:1.1

48.125W  
4.01A

35A  
38.5W



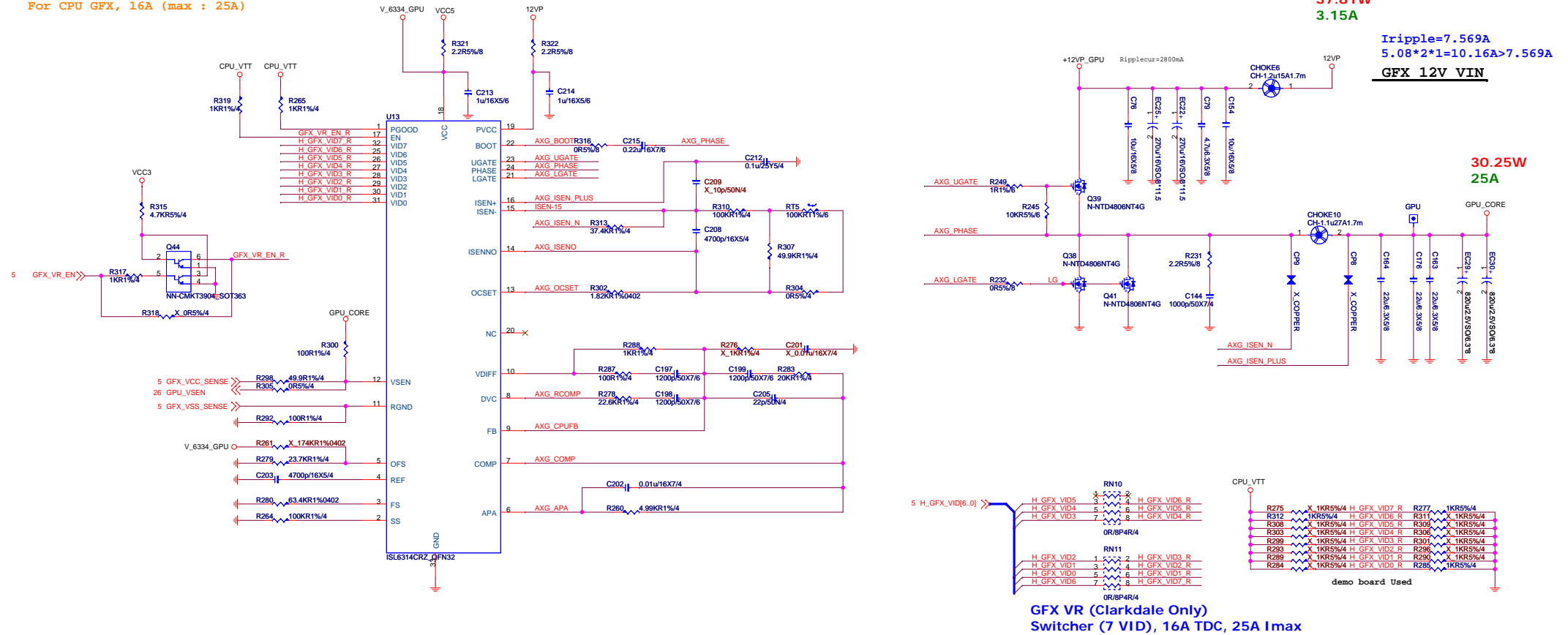
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## GPU\_CORE, 0.5V~1.3V S0

For CPU GFX, 16A (max : 25A)

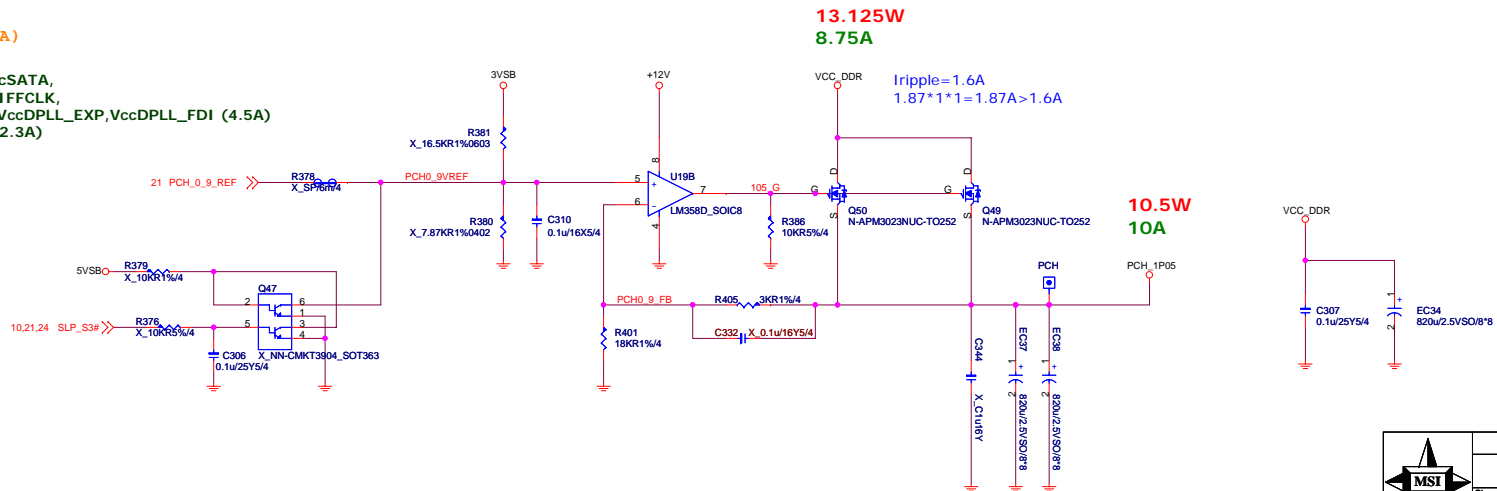


## PCH\_1P05, 1.05V

For PCH CORE, 4.5A (max : 7.5A)

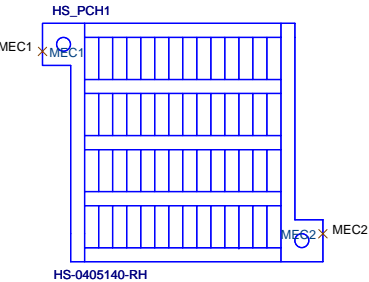
For PCH ME, 2.3A (max : 2.5A)

V1.05PCHS0: Vcc, VccExp, VccDMI, VccSATA, VccSATAPLL, VccAUPLL, VccSSC, VccDIFFCLK, VccDIFFCLKN, VccUSBCORE, VccDPLL, VccDPLL\_EXP, VccDPLL\_FDI (4.5A)  
V1.05MEM: VccMEW, VccAUX, VccME (2.3A)



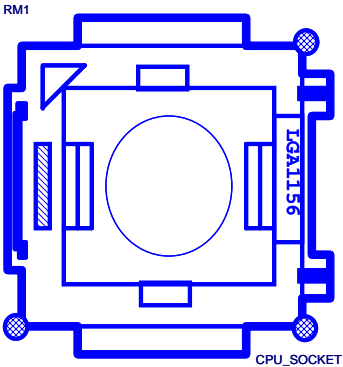


PCB

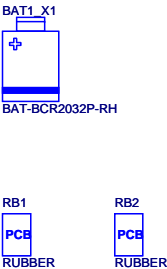


HEATPIPE

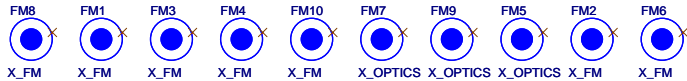
CPU SOCKET



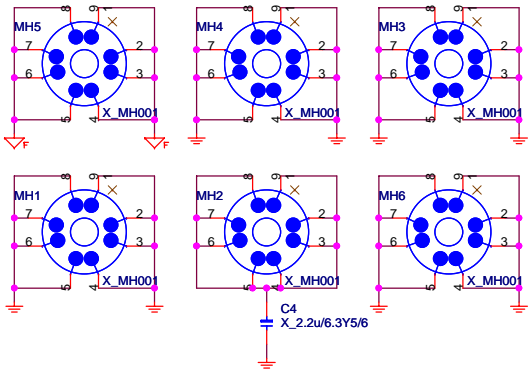
BATTERY



Optical Fiducial Marks-120



Mounting Holes



Simulation

